



ARM1136J(F)-S

A High-Performance, Low-Power Processor with DSP and Media Extensions

The award-winning ARM1136J-S™ and ARM1136JF-S™ processors deliver up to 660 Dhrystone 2.1 MIPS in a 0.13 μm process. Both processors feature the ARM v6 instruction set with media extensions, ARM Jazelle® technology for efficient embedded Java execution, ARM Thumb® code compression, and an optional floating-point coprocessor. Media processing extensions offer up to 1.9x the acceleration of media-processing tasks such as MPEG4 encode.

Instruction and data cache sizes are configurable, and optional Tightly Coupled Memories (TCMs) can be added to accelerate interrupt handling and data processing. These processors feature AMBA® 2.0 AHB™ interfaces compatible with a wide range of system IP and peripherals. The ARM1136JF-S processor also features an integrated floating-point coprocessor, which makes it particularly suitable for embedded 3D-graphics applications.

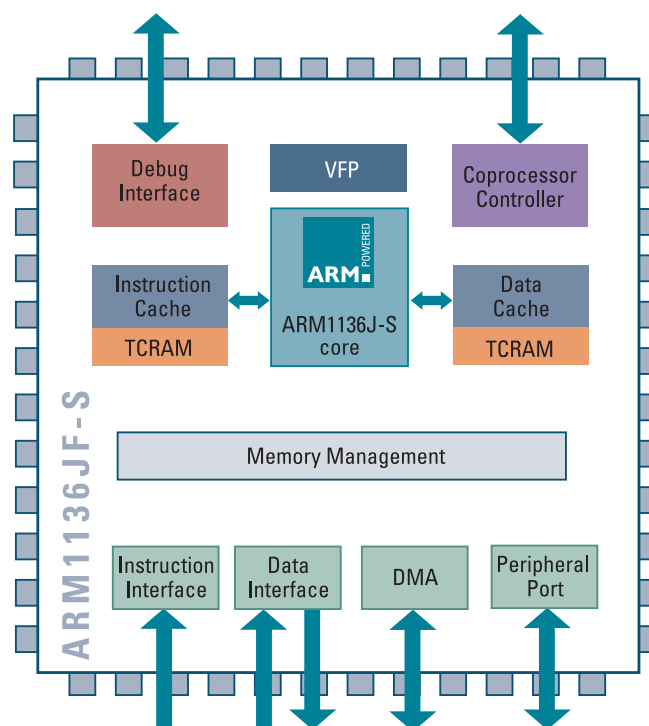
The ARM1136JF-S processor incorporates an integer unit that implements the ARM architecture v6. It supports the ARM and Thumb instruction sets, Jazelle technology to enable direct execution of Java bytecodes, and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

The ARM1136JF-S processor is a high-performance, low-power, ARM cached processor macrocell that provides full virtual memory capabilities.

Features ▶

- An integer unit with integral EmbeddedICE-RT logic
- An eight-stage pipeline
- Branch prediction with return stack
- Low-interrupt latency
- External coprocessor interface and coprocessors 14 and 15
- Instruction and Data Memory Management Units (MMUs), managed using MicroTLB structures backed by a unified Main TLB
- Instruction and data caches, including a non-blocking data cache with Hit-Under-Miss (HUM)
- The caches are virtually indexed and physically addressed, and have a 64-bit interface to both caches
- Level-one TCM that can be used as a local RAM with DMA, or as SmartCache
- High-speed Advanced Microprocessor Bus Architecture (AMBA) level two
- Vector Floating-Point (VFP) coprocessor support

In addition to the ARM1136J-S, ARM introduced a version that includes a VFP coprocessor. This is designated as the ARM1136JF-S.



Core ▶

The ARM1136JF-S processor is built around the ARM11 core in an ARMv6 implementation that runs the 32-bit ARM, 16-bit Thumb, and 8-bit Jazelle instruction sets. The processor contains EmbeddedICE-RT logic and a JTAG debug interface to enable hardware debuggers to communicate with the processor.

Registers ▶

The ARM1136JF-S core contains:

- 31 general-purpose 32-bit registers
- Seven dedicated 32-bit registers

Thumb Instruction Set ▶

Thumb is an extension to the ARM architecture. It contains a subset of the most commonly used 32-bit ARM instructions that has been encoded into 16-bit wide opcodes, to reduce memory requirements.

DSP Instructions ▶

The ARM DSP instruction set extensions provide the following:

- 16-bit data operations
- Saturating arithmetic
- Multiply Accumulate instructions (MAC)

Multiply instructions are processed using a single-cycle 32 x 16 implementation. There are 32 x 32, 32 x 16, and 16 x 16 multiply instructions.

Media Extensions ▶

The ARMv6 instruction set provides media instructions to complement the DSP instructions. The media instructions are divided into the following main groups:

- Additional multiplication instructions for handling 16-bit and 32-bit data, including dual-multiplication instructions that operate on both 16-bit halves of the source registers; this group includes an instruction that improves the performance and size of code for multi-word unsigned multiplications
- Instructions to perform Single Instruction Multiple Data (SIMD) operations on pairs of 16-bit values held in a single register, or on quadruplets of 8-bit values held in a single register; the main operations supplied are addition and subtraction, selection, pack, and saturation

Memory System ▶

The core provides a level-one memory system with the following features:

- Separate instruction and data caches
- Separate instruction and data RAMs
- 64-bit datapaths throughout the memory system
- Complete memory management
- 32-bit dedicated peripheral interface

Applications ▶

- Automotive infotainment: in-car entertainment, DVD players, and navigation equipment
- Networking: control processors in network infrastructure, switch, and router products
- Consumer: digital TVs, set-top boxes, game consoles, PDAs, and handheld digital media players

Core area, frequency range, and power consumption are dependent on process, libraries, and optimizations. The numbers quoted above are illustrative of synthesized cores using general-purpose TSMC process technologies and ARM Artisan standard-cell libraries and RAMs.

The speed-optimized implementations refer to the library choices and synthesis flow decisions and tradeoffs made in order to achieve the target frequency performance. The area-optimized implementations refer to the library choices and synthesis flow decisions and tradeoffs made in order to achieve a target area density.

The cache sizes are specified as InstructionCache/DataCache. The area without cache numbers quoted exclude RAM area, but include all logic including memory management, cache control, and debug. The area with cache numbers quoted includes the core, the specified instruction and data caches, and all necessary RAMs.

Performance Characteristics ▶	90 nm	
	Speed Optimized	Area Optimized
Standard cells	Advantage-HS	Metro
Memories	Advantage	Metro
Frequency* (MHz)	620	320
Area with cache (mm ²)	2.50	1.55
Area without cache (mm ²)	1.80	0.90
Cache size	16K/16K	16K/16K
Power with cache** (mW/MHz)	0.45	0.24
Power without cache** (mW/MHz)	0.37	0.18

*Worst-case conditions—0.18 μm process—1.62V, 125°C, slow silicon; 0.13 μm process—1.08V, 125°C, slow silicon; 90 nm process—0.9V, 125°C, slow silicon

**Typical-case conditions—0.18 μm process—1.8V, 25°C, typical silicon; 0.13 μm process—1.2V, 25°C, typical silicon; 90 nm process—1V, 25°C, typical silicon