



ARM Cortex-A8

Processors for Complex OS and User Applications

The ARM Cortex™-A8 processor is the first applications processor based on the ARMv7 architecture and is the highest performance, most power-efficient processor ever developed by ARM. With the ability to scale in speed from 600 MHz to greater than 1 GHz, the ARM Cortex-A8 processor can meet the requirements for power-optimized mobile devices needing operation in less than 300 mW and performance-optimized consumer applications requiring 2000 Dhrystone MIPS.

The ARM Cortex-A8 processor is ARM's first superscalar processor featuring technology for enhanced code density and performance, NEON™ technology for multimedia and signal processing, and Jazelle® RCT (Runtime Compilation Target) technology for efficient support of ahead-of-time and just-in-time compilation of Java and other bytecode languages.

The exceptional speed and power efficiency of the Cortex-A8 processor is enabled by new ARM Artisan® Advantage-CE libraries supporting and implementing advanced leakage control.

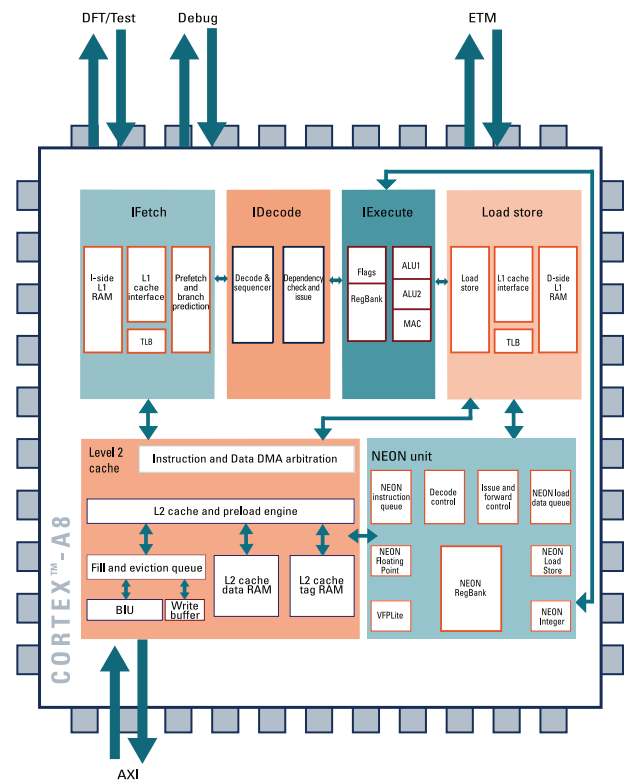
The processor is supported by a wide range of ARM technologies for rapid system design including:

- The RealView® DEVELOP family of software development tools
- The RealView CREATE family of ESL tools and models
- CoreSight™ debug and trace technology as well as software library support through the OpenMAX multimedia processing standard
- AMBA® 3 AXI high-performance SoC interconnect

Architectural Features ▶

The ARM Cortex-A8 processor's sophisticated pipeline architecture is based on dual, symmetric, in-order issue, 13-stage pipeline with advanced dynamic branch prediction achieving 2.0 DMIPS/MHz.

- The in-order, dual-issue, superscalar microprocessor core includes:
 - 13-stage main integer pipeline
 - Ten-stage NEON media pipeline
 - Dedicated Level 2 (L2) cache with programmable wait states
 - Global-history-based branch prediction
- The processor works in conjunction with a power-optimized load store pipeline to deliver 2.0 DMIPS/MHz for power-sensitive applications



- The ARM Cortex-A8 is ARMv7 architecture-compliant and includes:
 - Thumb®-2 technology for greater performance, energy efficiency, and code density
 - NEON signal processing extensions to accelerate media codecs such as H.264 and MP3
 - Jazelle RCT Java-acceleration technology to optimize Just In Time (JIT) and Dynamic Adaptive Compilation (DAC), and to reduce memory footprint by up to three times
 - TrustZone technology for secure transactions and Digital Rights Management (DRM)

- Integrated L2 cache:
 - Built using standard compiled RAMs
 - Configurable size from 64K to 2 MB
 - Programmable delay
- Optimized Level 1 (L1) cache:
 - Performance- and power-optimized
 - Combines minimal access latency with hash way determination to maximize performance and minimize power consumption
- Dynamic Branch Prediction:
 - Enabled by branch target and global-history buffers
 - Achieves 95 percent accuracy across industry benchmarks
 - Replay mechanism minimizes miss-predict penalty
- Memory system:
 - Single-cycle load-use penalty for access to the L1 cache
 - Hash array in the L1 cache limits activation of the memories to when they are likely to be needed
 - Direct interface between the integrated, configurable L2 cache and the NEON media unit for data streaming
 - Banked L2 cache design that enables only one bank at a time
 - Support for multiple outstanding transactions to the Level 3 (L3) memory to fully utilize the CPU

Performance Characteristics ▶	
	65 nm
	Speed Optimized
Frequency* (MHz)	600-800
Area with cache (mm ²)	<4
Area without cache (mm ²)	<3
Power with cache** (mW/MHz)	<0.5

*Core area, frequency range, and power consumption are dependent on process, libraries, and optimizations. The numbers quoted above are illustrative of synthesized cores using general-purpose TSMC process technologies and ARM Artisan standard-cell libraries and RAMs.

Area is for core only (excluding NEON, Trace technology, and L2 cache). Frequency and power are for mobile applications. Frequency for consumer applications = 1 GHz. The speed-optimized implementations refer to the library choices and synthesis flow decisions and tradeoffs made in order to achieve the target frequency performance. The area-optimized implementations refer to the library choices and synthesis flow decisions and tradeoffs made in order to achieve a target area density.

**The 65 nm (LP) dynamic power measured is at 1.2V nominal and, hence, is higher than the 65 nm (GP) dynamic power, which is at 1.0V. However, the 65 nm (LP) leakage is significantly lower and this is the major consideration for mobile or battery-operated devices that need to conserve power in standby mode.

