



## ARM966E-S

### Embedded Core with Flexible Memory System and DSP Instruction Set Extensions

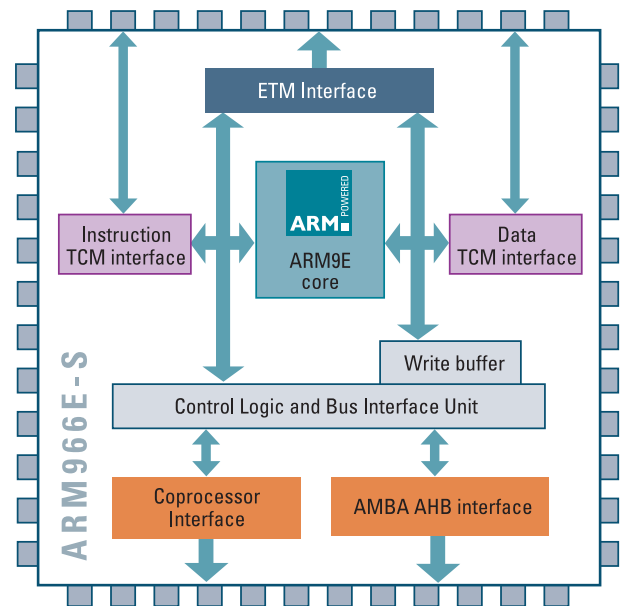
The ARM966E-S processor is targeted at a wide range of embedded applications where high performance, low system cost, small die size, and low power are all important. The ARM966E-S macrocell is a fully synthesizable 32-bit RISC processor aimed specifically at embedded hard real-time applications. The core

implements the ARMv5TE instruction set and features an enhanced 16- x 32-bit multiplier capable of single-cycle MAC operations, and 16-bit fixed point DSP instructions to accelerate signal processing algorithms and applications.

The ARM966E-S processor has separate, directly connected instruction and data Tightly Coupled Memory (TCM), which have flexible sizes and run at the processor clock speed. The ARM966E-S processor supports ARM's real-time trace technology with the optional ETM9 Embedded Trace Macrocell. The ARM966E-S features a simple memory map providing an area and power-efficient solution for applications that do not require complex memory management support. The core includes an AMBA AHB™ interface and a coprocessor interface for connection to application acceleration hardware such as the VFP9-S floating-point coprocessor.

The ARM966E-S processor provides a high-performance processor subsystem that includes the ARM9E-S RISC integer CPU core featuring:

- ARMv5TE 32-bit instruction set with improved ARM/Thumb code inter-working and enhanced multiplier designed for improved DSP performance
- ARM debug architecture with additional support for real-time debug; this enables critical exception handlers to execute while debugging the system
- Support for external TCM; a TCM interface is provided for each of the external instruction and data memory blocks; the TCM interfaces of the ARM966E-S processor enable high-speed operation without incurring the performance and power penalties of accessing the system bus, while having a lower area overhead than a cached memory system; the size of both the Instruction and Data TCM blocks are implementor-specific to enable tailoring of the hardware to the embedded application
- A simple fixed memory map for the local TCM, ideal for real-time embedded control applications



- An AMBA AHB bus interface
- Support for external coprocessors enabling floatingpoint or other application-specific hardware acceleration to be added
- Support for the use of a scan test methodology for the standard-cell logic and Built-In-Self-Test (BIST) for the TCM

Providing this complete high-frequency subsystem frees the SoC designer to concentrate on design issues unique to their system; the synthesizable nature of the device eases integration into ASIC technologies.

**Applications** ▶

- Automotive control: Powertrain with VFP9-S coprocessor
- Industrial control
- Motor control
- Mass storage devices: hard disc drives and DVD drives
- Networking systems
- Wireless devices
- Digital still cameras

**Features** ▶

- 32-/16-bit RISC architecture (ARMv5TE)
- 32-bit ARM instruction set for maximum performance and flexibility
- 16-bit Thumb instruction set for increased code density
- Tightly Coupled Memories (TCMs)
- EmbeddedICE-RT logic for real-time debug
- Floating point capability with VFP9-S coprocessor
- ETM interface for real-time trace capability with ETM9
- ARM-Synopsys Reference Methodology compliant deliverables
- Optional MOVE coprocessor delivers video encoding performance

**Benefits** ▶

- Single-chip MCU and DSP solution
- Deterministic performance from TCM memories
- Simple single-processor software structure; no need for software partitioning across MCUs and eliminates multi-MCU debugging
- Single development toolkit: reduced development costs and shorter development cycle time
- Optimized for hard real-time applications
- Multiple sourcing from industry-leading silicon vendors
- Code-compatible upward migration path to ARM10E family
- Excellent debug support for SoC designers
- Instruction set can be extended by the use of coprocessors
- ARM-EDA Reference Methodology deliverables significantly reduce the time to generate a specific technology implementation of the core and to generate industry-standard views and models

Core area, frequency range, and power consumption are dependent on process, libraries, and optimizations. The numbers quoted above are illustrative of synthesized cores using general-purpose TSMC process technologies and ARM Artisan standard-cell libraries and RAMs. The speed-optimized implementations refer to the library choices and synthesis flow decisions and tradeoffs made in order to achieve the target frequency performance. The area-optimized implementations refer to the library choices and synthesis flow decisions and tradeoffs made in order to achieve a target area density.

<b>Performance Characteristics</b> ▶				
	0.18 $\mu\text{m}$	0.13 $\mu\text{m}$	90 nm	
	Speed Optimized	Speed Optimized	Speed Optimized	Area Optimized
<b>Standard cells</b>	NA	NA	Advantage-HS	Metro
<b>Frequency* (MHz)</b>	200	250	500	250
<b>Area (mm<sup>2</sup>)</b>	2	1	0.70	0.35
<b>Power** (mW/MHz)</b>	0.70	0.25	0.15	0.07

\*Worst-case conditions—0.18  $\mu\text{m}$  process—1.62V, 125°C, slow silicon; 0.13  $\mu\text{m}$  process—1.08V, 125°C, slow silicon; 90 nm process—0.9V, 125°C, slow silicon

\*\*Typical-case conditions—0.18  $\mu\text{m}$  process—1.8V, 25°C, typical silicon; 0.13  $\mu\text{m}$  process—1.2V, 25°C, typical silicon; 90 nm process—1V, 25°C, typical silicon

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