ARM926EJ-S

Jazelle-Enhanced Macrocell Processor

The ARM926EJ-S™ fully synthesizable processor features a Jazelle-enhanced 32-bit RISC CPU, flexible size instruction and data caches, Tightly Coupled Memory (TCM) interfaces, and a Memory Management Unit (MMU). It also provides separate instruction and data AMBA AHB™ interfaces particularly suitable for multi-layer AHB-based systems. The ARM926EJ-S processor implements the ARMv5TEJ instruction set and includes an enhanced 16- x 32-bit multiplier, capable of single-cycle MAC operations. The instruction set includes 16-bit fixed-point DSP instructions to enhance performance of many signal processing algorithms and applications as well as supports Thumb® and Java byte code execution.

The ARM926EJ-S processor is a member of the ARM9 family of general-purpose microprocessors. The processor is targeted at multi-tasking applications where full memory management, high performance, small die size, and low power are all important.

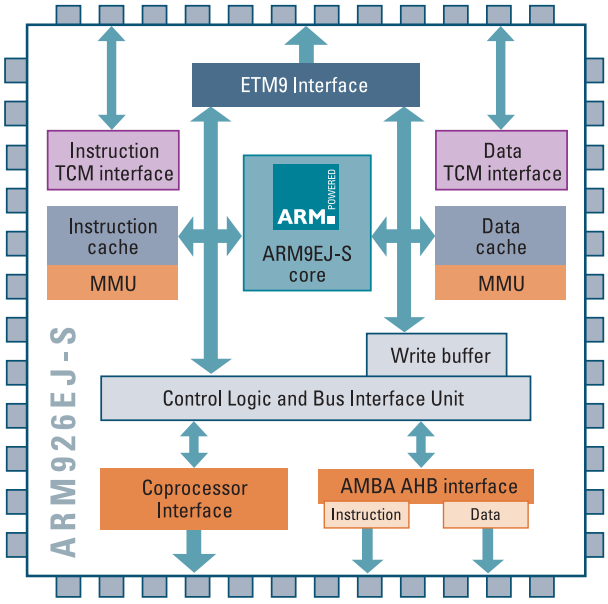
The processor supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density. The ARM926EJ-S processor includes features for efficient execution of Java byte codes, providing Java performance similar to JIT, but without the associated code overhead.

The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The processor has a Harvard cached architecture and provides a complete high-performance processor subsystem, including:

- An ARM9EJ-S integer core
- An MMU
- Separate instruction and data AMBA AHB bus interfaces
- Separate instruction and data TCM interfaces

The ARM926EJ-S processor provides support for external coprocessors, enabling the addition of other floating-point or other application-specific hardware acceleration. The processor implements ARM architecture version 5TEJ.

The ARM926EJ-S processor is a synthesizable macrocell. This means that you can optimize the macrocell for a particular target library, and you can configure the memory system to suit your target application. You can individually configure the cache sizes to be any power of two between 4 KB and 128 KB.



The tightly coupled instruction and data memories (TCM) are instantiated externally to the ARM926EJ-S macrocell, providing you with the flexibility to optimize the memory subsystem for performance, power, and particular RAM type. The TCM interfaces enable non-zero wait-state memory to be attached, as well as provide a mechanism for supporting DMA.

Applications ▸

- Automotive infotainment
- Audio and video decoding
- Platform OS-based devices
- Next-generation smart phones, communicators, and PDAs
- 3G baseband and applications processor
- Digital still camera

Features ▸

- 32/16-bit RISC architecture (ARMv5TEJ)
- 32-bit ARM instruction set for maximum performance and flexibility
- 16-bit Thumb instruction set for increased code density
- DSP instruction extensions and single-cycle MAC
- ARM Jazelle technology
- MMU which supports operating systems including Symbian OS, Windows CE, and Linux
- Flexible instruction and data cache sizes
- Instruction and data TCM interfaces with wait-state support
- EmbeddedICE-RT logic for real-time debug
- Industry-standard AMBA bus AHB interfaces
- ETM interface for real-time trace capability with ETM9
- Optional MOVE coprocessor delivers video encoding performance

Benefits ▸

- Runs all major OSs and existing middleware
- Single-chip MCU, DSP, and Java solution
- Support for leading Java run-times
- High-efficiency Java bytecode execution
- Ultra-low Java power consumption
- Java JIT compiler performance without the disadvantages
- Jazelle support code has no increase in VM size
- Simple single-processor software structure, no need for software partitioning across MCUs
- Single development toolkit for reduced development costs and shorter development cycle time
- Multiple sourcing from industry-leading silicon vendors
- Code-compatible upward migration path through to the latest cortex family of processors
- Process portable synthesizable design
- Excellent debug support for SoC designers
- Instruction set can be extended by the use of coprocessors
- ARM-EDA Reference Methodology deliverables significantly reduce the time to generate a specific technology implementation of the core and to generate industry-standard views and models

Performance Characteristics ▸

	0.18 µm	0.13 µm		90 nm	
	Speed Optimized	Speed Optimized	Area Optimized	Speed Optimized	Area Optimized
Standard cells	SAGE-X	SAGE-X	SAGE-X	Advantage-HS	Metro
Memories	HSHD	HSHD	HSHD	Advantage	Metro
Frequency* (MHz)	200	276	238	500	250
Area with cache (mm2)	6.5	2.78	2.39	1.55	0.85
Area without cache (mm2)	3	1.61	1.45	1.05	0.50
Cache size	8K/8K	8K/8K	8K/8K	8K/8K	8K/8K
Power with cache (mW/MHz)**	-	-	0.48	0.29	0.14
Power without cache (mW/MHz)**	-	-	0.36	0.24	0.11

*Worst-case conditions–0.18 µm process–1.62V, 125°C, slow silicon; 0.13 µm process–1.08V, 125°C, slow silicon; 90 nm process–0.9V, 125°C, slow silicon
**Typical-case conditions–0.18 µm process–1.8V, 25°C, typical silicon; 0.13 µm process–1.2V, 25°C, typical silicon; 90 nm process–1V, 25°C, typical silicon

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