



## ARM Cortex-M3

Processors Optimized for Cost-Sensitive and Deeply-Embedded Applications

The ARM Cortex™-M3 processor has been developed to provide a high-performance, low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

The ARM Cortex-M3 32-bit RISC processor executes purely Thumb®-2 instructions, delivering the high performance expected of an ARM core in the memory size usually associated with 8- and 16-bit devices; typically in the range of a few kilobytes of memory for microcontroller class applications.

In addition to minimizing its memory requirement, the ARM Cortex-M3 processor is also the smallest 32-bit core designed by ARM. This design reduces silicon area requirements even further, enabling the smallest of packages or the manufacturing of devices on low-cost processes, such as 0.35 μm and 0.25 μm.

The ARM Cortex-M3 processor also reduces the number of pins required for debug from five to one, by implementing a new debug interface technology—Single Wire Debug—that can replace the current multi-pin JTAG port.

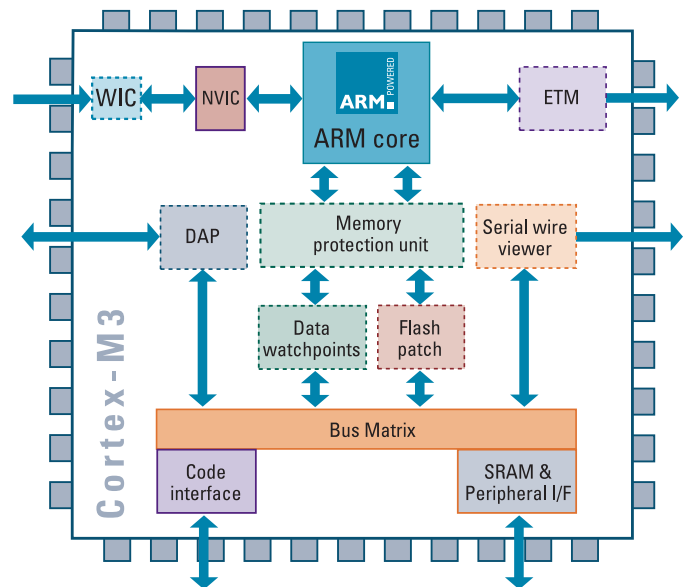
### Outstanding Performance ▶

In addition to unparalleled performance, power consumption, and memory utilization, the ARM Cortex-M3 processor also achieves exceptional interrupt handling. By implementing the register manipulations required for handling an interrupt in hardware, this core achieves minimal clock overhead on entering interrupts, and switches between pending or higher priority interrupts in only six cycles. The design, which comes with 32 interrupt channels as standard, can be configured to between one and over 240 channels.

The ARM Cortex-M3 processor also includes an optional Memory Protection Unit (MPU) to provide a privileged mode of operation for complex applications.

### Enabling Technology ▶

The ARM Cortex-M3 processor has been designed 'from the ground up' to provide optimal performance and power consumption within a minimal memory system. To achieve this, the core executes only the Thumb-2 instruction set, which delivers an unparalleled combination of ARM instruction set performance with industry-leading code density. The design, which is based on a three-stage pipeline Harvard architecture, also maximizes memory utilization through the support of unaligned data storage, and single-cycle atomic bit manipulation. The exceptional performance of the ARM Cortex-M3 processor is achieved through a highly revised architecture that also implements many new technologies in this type of core, such as hardware divide and single-cycle multiply.



**Benefits ▶**

The ARM Cortex-M3 processor offers significant benefits to system and software developers.

- Lower cost devices through smaller processing core, system, and memories
- Ultra-low power consumption and integrated sleep modes
- Outstanding processing performance for challenging applications
- Fast interrupt handling for critical control applications
- Platform security with optional integrated memory protection unit
- Enhanced system debug for faster development
- No assembler code requirement to ease system development
- Wide application envelope encompassing ultra-low-cost microcontrollers and high-performance SoC

Core area, frequency range, and power consumption are dependent on process, libraries, and optimizations. The numbers quoted in the table below are illustrative of synthesized cores using general-purpose TSMC process technologies and ARM Artisan® standard-cell libraries and RAMs. Area numbers include the CM3Core, the Nested Vectored Interrupt Controller (NVIC), and Bus Matrix, but not the optional components including the Memory Protection Unit, Embedded Trace Macrocell, Breakpoint Unit, Data Watchpoint Unit, and Trace Port Interface Unit.

The speed-optimized implementations refer to the library choices and synthesis flow decisions and tradeoffs made in order to achieve the target frequency performance. The area-optimized implementations refer to the library choices and synthesis flow decisions and tradeoffs made in order to achieve a target area density.

Performance Characteristics ▶						
	0.18 $\mu\text{m}$		0.13 $\mu\text{m}$		90 nm	
	Speed Optimized	Area Optimized	Speed Optimized	Area Optimized	Speed Optimized	Area Optimized
Standard cells	Metro	Metro	SAGE-X	Metro	Advantage	Advantage
Frequency* (MHz)	100	50	135	50	191	50
CM3Core area (mm <sup>2</sup> )	0.43	0.35	0.43	0.21	0.21	0.13
CM3Core power** (mW/MHz)	0.31	0.21	0.14	0.07	0.07	0.04
Area (mm <sup>2</sup> )	0.78	0.64	0.74	0.38	0.37	0.25
Power** (mW/MHz)	0.37	0.25	0.165	0.084	0.083	0.047

\*Worst case conditions—0.18  $\mu\text{m}$  process—1.62V, 125°C, slow silicon; 0.13  $\mu\text{m}$  process—1.08V, 125°C, slow silicon

\*\*Typical case conditions—0.18  $\mu\text{m}$  process—1.8V, 25°C, typical silicon; 0.13  $\mu\text{m}$  process—1.2V, 25°C, typical silicon

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