

Things to consider Pinning Out Your PSOC

By Larry Carleton AE Arrow Electronics Engineering Solution Center



Table of Contents

How to Pin Out your PSOC	4
Analog pin Out:	4
Digital pin Out:	5
Device Pin Out Listings	7
CY8C201XX	7
CY8C20110-LDX2I	7
CY8C20110-SX2I.....	8
CY8C20X34	8
CY8C20234 16 Pin QFN	8
CY8C20334 24 Pin QFN	9
CY8C20434 32 Pin QFN	9
CY8C20X46, CY8C20X66	9
CY8C20246 CY8C20466 16 Pin QFN.....	10
CY8C20346 CY8C20466 24 Pin QFN.....	10
CY8C20446 CY8C20466 32 Pin QFN.....	11
CY8C20546 CY8C20566 48 Pin SSOP	11
CY8C20666 48 Pin QFN.....	12
CY8C20066 48 Pin QFN OCD(on chip debugger Not for Production).....	12
CY8C21X23	13
CY8C21123 8 Pin PSoC Device SOIC	13
CY8C21223 16-Pin PSoC Device SOIC	13
CY8C21323 20-Pin PSoC Device SSOP.....	13
CY8C21323 24-Pin PSoC Device MFL pkg.....	14
CY8C21X34	14
CY8C21234 16-Pin (SOIC).....	14
CY8C21334 20-Pin (SSOP)	15
CY8C21534 28-Pin (SSOP)	15
CY8C23X33	16
CY8C23533 32-Pin PSoC Device QFN	16
CY8C23433 28-Pin PSoC Device SSOP.....	17
CY8C24X23A	18
CY8C24123A 8-Pin PSoC Device PDIP and SOIC.....	18
CY8C24223A 20-Pin PSoC Device PDIP, SSOP, and SOIC	18
CY8C24423A 28-Pin PSoC Device PDIP, SSOP, and SOIC	19
CY8C24423A 32-Pin PSoC Device 32-Pin QFN or Sawn	20
CY8C24000A 56-Pin PSoC Device	20
CY8C24X94	20
CY8C24794 56-Pin PSoC Device QFN	21
CY8C24894 56-Pin PSoC Device QFN	22
CY8C24994 68-Pin PSoC Device QFN	23
CY8C24094 68-Pin OCD PSoC Device QFN.....	23
CY8C24094 On-Chip Debug (OCD) device 100-pin VFBGA not for production..	24
CY8C27X43	25
CY8C27143 8-Pin PSoC Device PDIP.....	25
CY8C27243 20-Pin PSoC Device (SSOP, SOIC).....	26

CY8C27443 28-Pin PSoC Device (PDIP, SSOP, SOIC)	27
CY8C27543 44-Pin PSoC Device (TQFP).....	28
CY8C27643 48-Pin PSoC Device (SSOP).....	29
CY8C27643 48-Pin PSoC Device (QFN).....	30
CY8C27002 56-Pin ODC PSoC Device (SSOP).....	31
CY8C29X66	32
CY8C29466 28-Pin PSoC Device (PDIP, SSOP, SOIC)	32
CY8C29566 44-Pin PSoC Device (TQFP).....	33
CY8C29666 48-Pin PSoC Device (SSOP).....	34
CY8C29666 48-Pin PSoC Device (QFN).....	35
CY8C29866 100-Pin PSoC Device (TQFP).....	36
CY8C29000 On-Chip Debug (OCD) PSoC device	37

How to Pin Out your PSOC

This Application Note is intended to facilitate your layout before you are done writing your code. The devices listed below are covered in this document. A chronological list of all the PSOC device pin outs and packages with the pin functions and alternate functions is contained at the end of this document. A brief description of the device family is also given at the beginning of each subsection. The family part numbers below are covered in this document.

CY8C201XX, CY8C20X34, CY8C20X46, CY8C20X66, CY8C21X23, CY8C21X34, CY8C23X33, CY8C24X23A, CY8C24X94, CY8C27X43, CY8C29X66

Basic PSOC guidelines for pinning out your PSOC

Every PSOC data sheet has a pin out figure for the PSOC devices. These diagrams have port and pin number information along with a table that shows all the possible functions a pin can have. Below is the legend for the pin out definition table for a CY8C20XXX parts.

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output. CY8C20XXX parts.

Note that in the legend above there are 5 different possible pin functions. These functions are shown in the pin definition table in each data sheet for each part and package. The legend may differ for each family of parts, as new features and performance levels have been added to the PSOC over the last several years.

Analog pin Out:

Two columns are provided in the pin out definitions, digital and analog. One important thing to keep in mind is the analog functional pin out that may be required for the project. The reason this is important is the analog inputs and outputs are dedicated to one or two ports in most parts. Use the analog block diagram as seen in figure 1 to decide on which pins you would like to use. Figure 1 is the analog block diagram for the CY8C27X43 series of parts. The first and easiest thing to see in the block diagram is that four pins can be used for analog output pins. The pins are P0[5], P0[4], P0[3], and P0[2]. These pins have dedicated drivers that can be enabled for outputting analog signals from the analog blocks sections. Each analog column has a dedicated buffer that can be enabled to drive an analog signal output. Look at figure 2 and the buffer amps are at the bottom, labeled buf0, buf1, buf2, and buf3. The CY8C27X43 parts have 4 columns of analog blocks. Each column has a buffer to buffer any of the three analog blocks in that column to the output pin, see figure 2 showing the analog blocks in Designer. Only one analog block output in the column can be directly connected to the output pin. Analog column 1 is output on pin P0[3], analog column 2 is output on pin P0[5], analog column 3 is output on pin P0[4], and analog column 4 is output on pin P0[2]. Because these buffers are dedicated to a specific analog column the customer should pull in the analog user blocks that he is planning to use. Connect the blocks using the chip view in Designer and make sure you can connect the block you want to the analog output pin

desired. Left clicking on any of the buf outputs will show you the port pins that it can be connected too.

Analog inputs are forced to be on port 0 and port 2, see figure 1.. Port 0 odd pins connect to a 4 to 1 mux(ACI0) that can be set to input 1 of the 4 odd pins to analog column 0 analog blocks. These port 0 odd pins are also routed to another 4 to 1 mux(ACI1) that can be set to input 1 of the 4 odd pins to analog column 2 analog blocks. The same is true for the port 0 even pins. Figure 1. is very accurate and can and should be verified using designer when hooking up analog input signals. Left clicking on any of the 4 to 1 mux symbols in Designer as seen in figure 2. will show the user which port pins can be connected to the input of the mux. When multiple analog inputs need to be input to one particular block be sure that the signals can be routed to the appropriate analog 4 to 1 mux block. In Designer pulling in a 4 to 1 mux uses no analog blocks but does use whichever 4 to 1 mux that is set in the configuration window for the mux. The API for the 4 to 1 mux user module gives the user the ability to change the mux dynamically in the software. Port 2 has direct connections to switched capacitor(SC) blocks as seen in figure 2.. A generic SC user module has two inputs. If the module is placed in either the middle left or right bottom SC block as in figure 2 then direct connections can be made using either P2[3] and P2[1] if the left middle block is used or using P2[2] and P2[0] if the right bottom SC block is used. Port 2 also has additional analog input functionality on pins P2[4] and P2[6] which allows the user to input an external voltage reference and or an analog ground reference into the PSOC if desired. Different PSOC families have slightly different setups for inputting and outputting analog signals. Be sure to look closely at the analog block diagram of the part of interest, along with using the chip view in Designer to verify your pin out before going to layout for your design. If multiple signals are to be multiplexed to a single analog block the user library contains both a 4 to 1 and 8 to 1 mux user modules that should be used. Be sure and use the Designer tool to connect up these mux modules before committing to layout if the designer desires this functionality. Placing user modules and hooking them up to the outside pins of the device can be done very fast. This should be done before committing the design to layout to verify the correct connections can be made.

Digital pin Out:

Digital signal inputs and outputs are much more versatile. All port pins can be either digital input or output pins. Some of the older parts have different drive capabilities on the outputs. This will be noted in the data sheet for each family of parts. Some special digital functional sources have dedicated output pins. This includes the ISSP(in system serial programming) programming pins along with the built in I2C hardware pins. P1[1] is always used as the ISSP clock pin if in circuit programming is going to be used in the design. P1[0] is the data pin for ISSP connection and like P1[1] will not be high impedance during power on reset. Most PSOC devices have a built in I2C digital system that also use P1[0 and 1] pins. The I2C system uses these two pins for the interface to the I2C hardware in the PSOC.

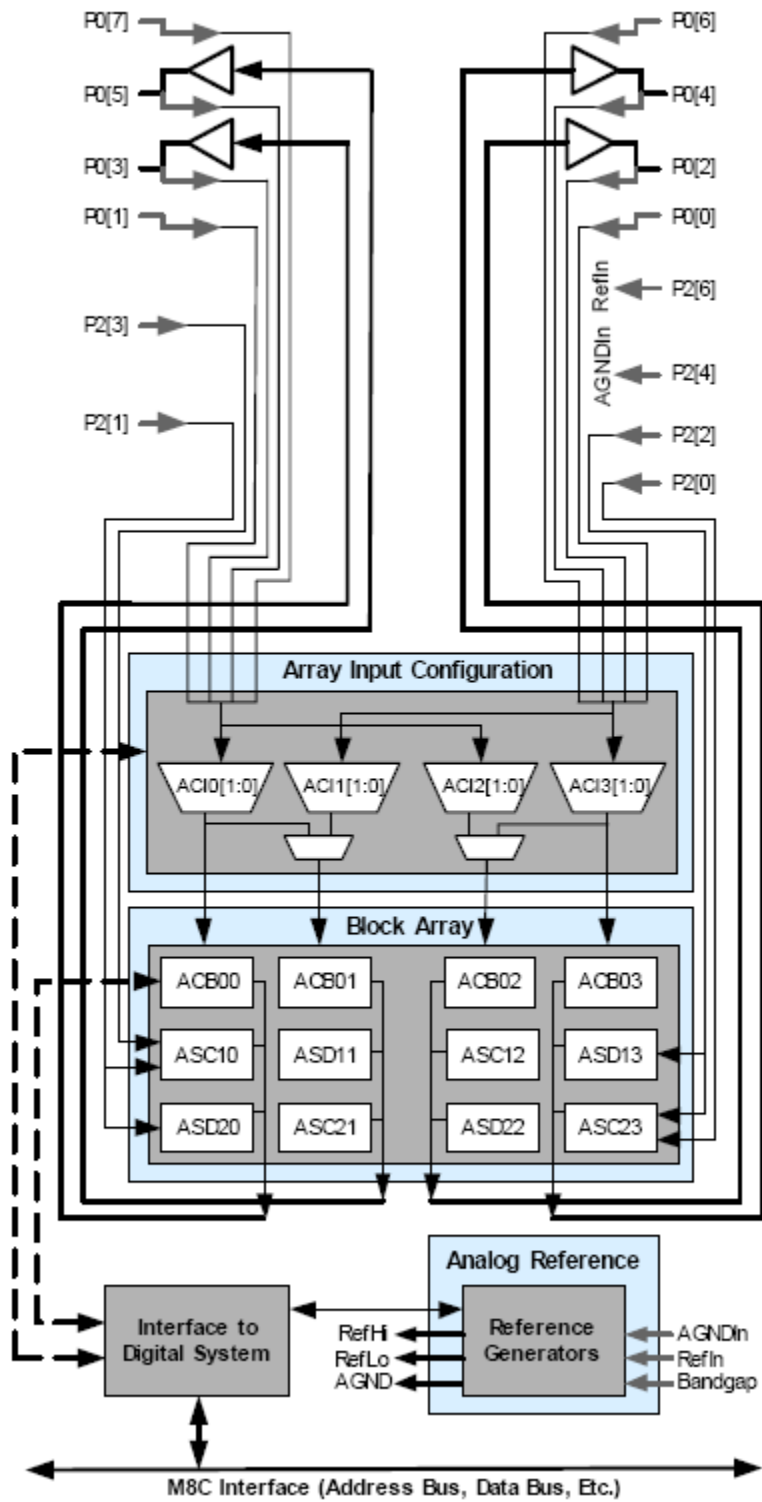


Figure 1. CY8C27X43 Analog block diagram

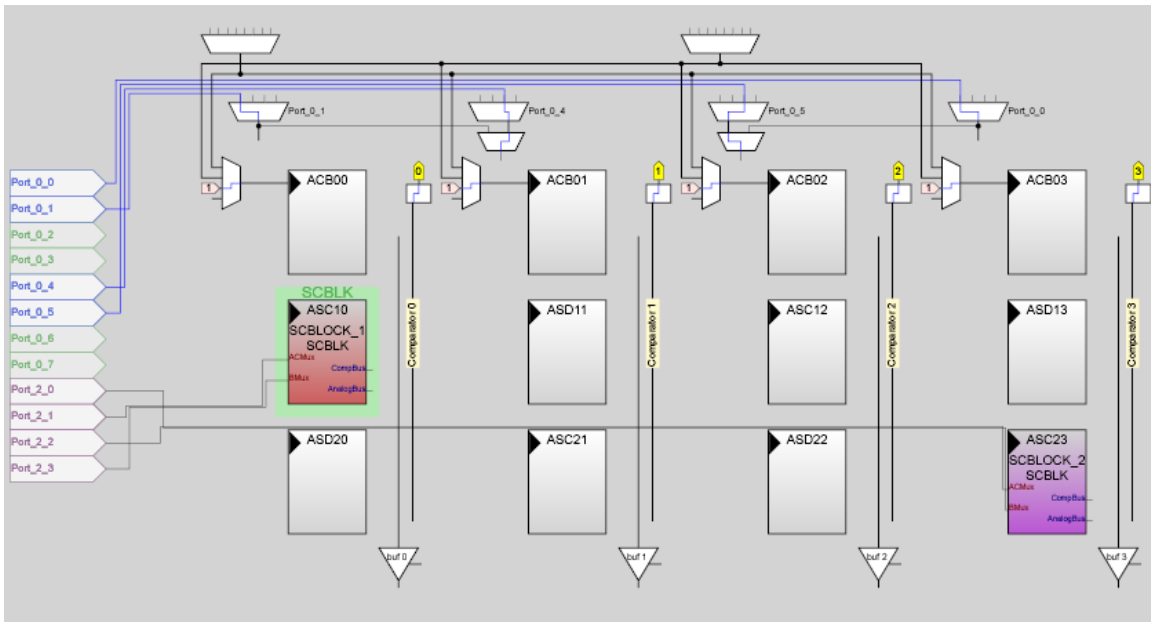


Figure 2. Analog Blocks CY27x43 parts

Figure 2. Analog Blocks CY8C27x43 parts view in Designer

Device Pin Out Listings

Below is a set of tables that covers the pin out functions of most of the PSoC devices. All parts are listed chronologically. A short description of the base part is given along with a list of the dedicated pins for each device and a second table listing pins with possible alternate functions.

CY8C201XX

Cap Sense parts have 10 cap sense I/O that can be used as cap sense buttons or slider pins or general purpose I/O. The parts also have dedicated ISSP (In circuit serial programming) data and clock pins along with power (VDD) and ground (VSS) pins and reset. These pins are all dedicated and can not be moved. The I2C pins, are not High Z at POR (Power On Reset).

These parts come in two 16 pin packages.

CY8C20110-LDX2I

The COL (QFN) package has six dedicated pins for ISSP, power and ground, and integrating capacitor connections.

Pin	VCC	GRD	ISSP	Cint	Reset	CapSense or GPIO
	13	7	3,4	15	11	Port 0(1,2,12,14,16) Port 1(5,6,9,10)

CY8C20110-SX2I

The SOIC package has six dedicated pins for ISSP, power, ground, reset, and integrating capacitor connections.

	VCC	GRD	ISSP	Cint	Reset	CapSense or GPIO
Pin	16	10	6,7	2	14	Port 0(1,3,4,5,15) Port 1(8,9,11,12,13)

CY8C20X34

Cap sense parts have up to 28 cap sense I/O depending on the package. The parts also have dedicated I2C pins used for ISSP and I2C communications. The device also has a 4 wire SPI function that shares the I2C pins. The QFN 16 pin CY8C20234 part has some dedicated pins for ISSP programming that are shared depending on what the customer wants. Dedicated pins are listed below. This series of PSOC has an on board LDO that can be programmed to different voltages depending on the customer needs. The output of the LDO is used to regulate the output voltages on port 1 of the PSOC to interface to lower voltage level parts in the design. The LDO can be disabled allowing port 1 to run at the PSOC nominal supply levels.

CY8C20234 16 Pin QFN

	VDD	GRD	ISSP	Cint	Reset	CapSense or GPIO
Pin	13	7	6,8	15	11	Port 0(16,15,14,12) Port 1(8,6,9,5,10,4,3) Port 2(2,1)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2nd Alternate
3-P1[7]	I/O	I2C SCL	SPI SS
4-P1[5]	I/O	I2C SDA	SPI MISO
5-P1[3]	I/O	SPI CLK	
6-P1[1]	ISSP CLK*	I2C SCL	SPI MOSI
8-P1[0]	ISSP DATA*	I2C SDA	
10-P1[4]	I/O	EXT CLK IN	
15-P0[3]	I/O	Integrating Input(Cint)	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C20334 24 Pin QFN

Pin	VDD	GRD	ISSP	Cint	Reset	CapSense or GPIO
	20	9	7,10	23	14	Port 0(16,24,17,23,18,22,19,21) Port 1(10,7,11,6,12,5,13,4) Port 2(15,3,2,1)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
4-P1[7]	I/O	I2C SCL	SPI SS
5-P1[5]	I/O	I2C SDA	SPI MISO
6-P1[3]	I/O	SPI CLK	
7-P1[1]	ISSP CLK*	I2C SCL	SPI MOSI
10-P1[0]	ISSP DATA*	I2C SDA	
12-P1[4]	I/O	EXT CLK IN	
23-P0[3]	I/O	Integrating Input(Cint)	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C20434 32 Pin QFN

Pin	VDD	GRD	ISSP	Cint	Reset	CapSense or GPIO
	28	32,12	11,13	31	17	Port 0(24,1,25,31,26,30,27,29) Port 1(13,11,14,10,15,9,16,8) Port 2(20,5,21,4,22,3,23,2) Port 3(18,7,19,6)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
8-P1[7]	I/O	I2C SCL	SPI SS
9-P1[5]	I/O	I2C SDA	SPI MISO
10-P1[3]	I/O	SPI CLK	
11-P1[1]	ISSP CLK*	I2C SCL	SPI MOSI
13-P1[0]	ISSP DATA*	I2C SDA	SPI CLK
15-P1[4]	I/O	EXT CLK IN	
31-P0[3]	I/O	Integrating Input(Cint)	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C20X46, CY8C20X66

These parts are Cap sense parts with 16K and 32K of flash respectively.

The architecture for this device family is comprised of three main areas: the Core, the CapSense Analog System, and the System Resources (including a full-speed USBport, CY8C20666 part only). A common, versatile bus allows connection between IO and the analog system. Each CY8C20x46/CY8C20x66 PsoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive

sensing applications. Depending on the PSoC package, up to 36 general purpose IO (GPIO) are also included. A built in LDO is included so that port 1 output logic levels can be programmed to match existing voltage levels in the system.

CY8C20246 CY8C20466 16 Pin QFN

	VDD	GRD	ISSP	Cint	Reset	CapSense or GPIO
Pin	13	7	6,8	15	11	Port 0(16,15,14,12) Port 1(8,6,9,5,10,4,3) Port 2(2,1)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
3-P1[7]	I/O	I2C SCL	SPI SS
4-P1[5]	I/O	I2C SDA	SPI MISO
5-P1[3]	I/O	SPI CLK	
6-P1[1]	ISSP CLK*	I2C SCL	SPI MOSI
8-P1[0]	ISSP DATA*	I2C SDA	SPI CLK
10-P1[4]	I/O	EXT CLK IN	
15-P0[3]	I/O	Integrating Input(Cint)	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C20346 CY8C20466 24 Pin QFN

	VDD	GRD	ISSP	Cint	Reset	CapSense or GPIO
Pin	20	9	7,10	23	14	Port 0(16,24,17,23,18,22,19,21) Port 1(10,7,11,6,12,5,13,4) Port 2(15,3,2,1)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P2[5]	I/O	Crystal Out	
2-P3[3]	I/O	Crystal In	
4-P1[7]	I/O	I2C SCL	SPI SS
5-P1[5]	I/O	I2C SDA	SPI MISO
6-P1[3]	I/O	SPI CLK	
7-P1[1]	ISSP CLK*	I2C SCL	SPI MOSI
10-P1[0]	ISSP DATA*	I2C SDA	SPI CLK
12-P1[4]	I/O	EXT CLK IN	
23-P0[3]	I/O	Integrating Input(Cint)	
24-P0[1]	I/O	Integrating Input(Cint)	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C20446 CY8C20466 32 Pin QFN

Pin	VDD	GRD	ISSP	Cint	Reset	CapSense or GPIO
	28	32,12	11,13	1,31	17	Port 0(24,1,25,31,26,30,27,29) Port 1(13,11,14,10,15,9,16,8) Port 2(20,5,21,4,22,3,23,2) Port 3(18,7,19,6)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[1]	I/O	Integrating Input(Cint)	
3-P2[5]	I/O	Crystal Out	
4-P2[3]	I/O	Crystal In	
8-P1[7]	I/O	I2C SCL	SPI SS
9-P1[5]	I/O	I2C SDA	SPI MISO
10-P1[3]	I/O	SPI CLK	
11-P1[1]	ISSP CLK*	I2C SCL	SPI MOSI
13-P1[0]	ISSP DATA*	I2C SDA	SPI CLK
15-P1[4]	I/O	EXT CLK IN	
31-P0[3]	I/O	Integrating Input(Cint)	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C20546 CY8C20566 48 Pin SSOP

Pin	VDD	GRD	ISSP	Cint	Reset	CapSense or GPIO
	48	24	23,25	31	17	Port 0(44,4,45,3,46,2,47,1) Port 1(25,23,26,22,27,21,28,20) Port 2(40,8,41,7,42,6,43,5) Port 3(36,17,37,16,38,15,39,14) Port 4(12,11)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
3-P0[3]	I/O	Integrating Input(Cint)	
4-P0[1]	I/O	Integrating Input(Cint)	
6-P2[5]	I/O	Crystal Out	
7-P2[3]	I/O	Crystal In	
20-P1[7]	I/O	I2C SCL	SPI SS
21-P1[5]	I/O	I2C SDA	SPI MISO
22-P1[3]	I/O	SPI CLK	
23-P1[1]	ISSP CLK*	I2C SCL	SPI MOSI
25-P1[0]	ISSP DATA*	I2C SDA	SPI CLK
27-P1[4]	I/O	EXT CLK IN	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C20666 48 Pin QFN

	VDD	GRD	ISSP	Cint	Reset	USB	CapSense or GPIO
Pin	21,41	18,47	17,22	46,48	26	19,20	Port 0(37,48,38,46,39,45,40,44) Port 1(22,17,23,16,24,13,25,12) Port 2(33,5,34,4,35,3,36,2) Port 3(27,11,28,10,29,9,30,8) Port 4(31,7,32)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
3-P2[5]	I/O	Crystal Out	
4-P2[3]	I/O	Crystal In	
12-P1[7]	I/O	I2C SCL	SPI SS
13-P1[5]	I/O	I2C SDA	SPI MISO
16-P1[3]	I/O	SPI CLK	
17-P1[1]	ISSP CLK*	I2C SCL	SPI MOSI
22-P1[0]	ISSP DATA*	I2C SDA	SPI CLK
24-P1[4]	I/O	EXT CLK IN	
46-P0[3]	I/O	Integrating Input(Cint)	
48-P0[1]	I/O	Integrating Input(Cint)	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C20066 48 Pin QFN OCD(on chip debugger Not for Production)

This is a debugging IC intended for development debugging. The pin out is the same as the above CY8C20666 with the addition of 3 debugging pins which are no connects on the production part. The three pins are listed below. Pin 1 OCDOE OCD mode direction pin. Pin 42 OCDE OCD even data IO. Pin 43 OCDO OCD odd data IO.

CY8C21X23

Each PSoC device includes four digital blocks. Depending on the PSoC package, up to two analog comparators and up to 16 general purpose IO (GPIO) are also included. The GPIO provide access to the global digital and analog interconnects. A switch mode power supply is also available on certain devices allowing the part to run on voltages as low as 1.0 volt. All port 0 pins can be digital I/O or analog inputs to analog input mux.

CY8C21123 8 Pin PSoC Device SOIC

	VDD	GRD	ISSP	GPIO
Pin	8	4	3,5	Port 0(6,2,7,1) Port 1(5,3)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate
3-P1[1]	ISSP CLK*	I2C CLK
5-P1[0]	ISSP DATA*	I2C Data

CY8C21223 16-Pin PSoC Device SOIC

	VDD	GRD	ISSP	SMP	GPIO
Pin	16	6	7,9	5	Port 0(12,4,13,3,14,2,15,1) Port 1(9,7,10,11)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate
7-P1[1]	ISSP CLK	I2C CLK
9-P1[0]	ISSP DATA	I2C Data
11-P1[4]	I/O	EXT CLK IN

CY8C21323 20-Pin PSoC Device SSOP

	VDD	GRD	ISSP	SMP	Reset	GPIO
Pin	20	5,10	9,11	NA	15	Port 0(16,4,17,3,18,2,19,1) Port 1(11,9,12,8,13,7,14,6)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate
6-P1[7]	I/O	I2C CLK
7-P1[5]	I/O	I2C Data
9-P1[1]	ISSP CLK*	I2C CLK
11-P1[0]	ISSP DATA*	I2C Data
13-P1[4]	I/O	EXT CLK IN

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C21323 24-Pin PSoC Device MLF pkg

	VDD	GRD	ISSP	SMP	Reset	GPIO
Pin	20	3,9,21	7,10	2	14	Port 0(16,1,17,24,18,23,19,22) Port 1(10,7,11,6,12,5,13,4)

Some pins have shared resources that may be configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate
4-P1[7]	I/O	I2C CLK
5-P1[5]	I/O	I2C Data
7-P1[1]	ISSP CLK*	I2C CLK
10-P1[0]	ISSP DATA*	I2C Data
12-P1[4]	I/O	EXT CLK IN

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C21X34

Configurable global bus resources allow combining all the device resources into a complete custom system. Each CY8C21x34 PSoC device includes four digital blocks and four analog blocks. Depending on the PSoC package, up to 28 general purpose IO (GPIO) are also included. The GPIO provide access to the global digital and analog interconnects.

CY8C21234 16-Pin (SOIC)

	VDD	GRD	ISSP	SMP	GPIO
Pin	16	6,8	7,9	5	Port 0(12,4,13,3,14,2,15,1) Port 1(9,7,10,11)

Some pins have shared resources that may be configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate
3-P0[3]	I/O	Integrating Input
4-P0[1]	I/O	Integrating Input
7-P1[1]	ISSP CLK*	I2C CLK
9-P1[0]	ISSP DATA*	I2C Data
11-P1[4]	I/O	EXT CLK IN

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C21334 20-Pin (SSOP)

	VDD	GRD	ISSP	SMP	Reset	GPIO
Pin	20	5,10	9,11	NA	15	Port 0(16,4,17,3,18,2,19,1) Port 1(11,9,12,8,13,7,14,6)

Some pins have shared resources that may be configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate
3-P0[3]	I/O	Integrating Input
4-P0[1]	I/O	Integrating Input
6-P1[7]	I/O	I2C CLK
7-P1[5]	I/O	I2C Data
9-P1[1]	ISSP CLK*	I2C CLK
11-P1[0]	ISSP DATA*	I2C Data
13-P1[4]	I/O	EXT CLK IN

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C21534 28-Pin (SSOP)

	VDD	GRD	ISSP	SMP	Reset	GPIO
Pin	28	14,9	13,15	NA	19	Port 0(24,4,25,3,26,2,27,1) Port 1(15,13,16,12,17,11,18,10)

Some pins have shared resources that may be configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate
3-P0[3]	I/O	Integrating Input
4-P0[1]	I/O	Integrating Input
6-P1[7]	I/O	I2C CLK
7-P1[5]	I/O	I2C Data
9-P1[1]	ISSP CLK*	I2C CLK
11-P1[0]	ISSP DATA*	I2C Data
13-P1[4]	I/O	EXT CLK IN

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C23X33

The PSoC CY8C23x33 family can have up to three IO ports that connect to the global digital and analog interconnects, providing access to four digital blocks and four analog blocks. A preconfigured 8 bit SAR ADC is present with conversion rates as fast as 2.7uS. Up to 10 different inputs can be multiplexed to the ADC input.

CY8C23533 32-Pin PSoC Device QFN

	VDD	GRD	ISSP	Reset	CapSense or GPIO
Pin	28	12	11,13	18	Port 0(23,32,24,31,26,30,27,29) Port 1(13,11,14,10,15,8,17,7) Port 2(19,4,20,3,21,2,22,1)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
3-P2[3]	I/O	Analog Column In	Direct SC Blk In
4-P2[1]	I/O	Analog Column In	Direct SC Blk In
5-P3[0]	I/O	Analog ADC Ref In	
7-P1[7]	I/O	I2C SCL	
8-P1[5]	I/O	I2C SDA	
11-P1[1]	ISSP CLK*	I2C SCL	XTALin
13-P1[0]	ISSP DATA*	I2C SDA	XTALout
15-P1[4]	I/O	EXT CLK IN	
19-P2[0]	I/O	Direct SC Blk In	
20-P2[2]	I/O	Direct SC Blk In	
21-P2[4]	I/O	Analog Grd Ref	
22-P2[6]	I/O	Ext Vref	
23-P0[0]	I/O	Analog column In	ADC In
24-P0[2]	I/O	Analog column In	ADC In
26-P0[4]	I/O	Analog column In	ADC In
27-P0[6]	I/O	Analog column In	ADC In
29-P0[7]	I/O	Analog column In	ADC In
30-P0[5]	I/O	Analog column In/Out,	ADC In
31-P0[3]	I/O	Analog column In/Out	ADC In
32-P0[1]	I/O	Analog column In	ADC In

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C23433 28-Pin PSoC Device SSOP

Pin	VDD	GRD	ISSP	Reset	CapSense or GPIO
	28	14	13,15	N/A	Port 0(24,4,25,3,26,2,27,1)
					Port 1(15,13,16,12,17,11,18,10)
					Port 2(20,8,21,7,22,6,23,5)
					Port3(9,19)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[7]	I/O	Analog Column In	ADC In
2-P0[5]	I/O	Analog Column In/Out	ADC In
3-P0[3]	I/O	Analog Column In/Out	ADC In
4-P0[1]	I/O	Analog Column In	ADC In
7-P2[3]	I/O	SC BLK In	
8-P2[1]	I/O	SC BLK In	
9-P3[0]	I/O	ADC Ref Option	
10-P1[7]	I/O	I2C SCL	
11-P1[5]	I/O	I2C SDA	
13-P1[1]	ISSP CLK*	I2C SCL	XTALin
15-P1[0]	ISSP DATA*	I2C SDA	XTALout
17-P1[4]	I/O	Ext Clk In	
20-P2[0]	I/O	SC BLK In	
21-P2[2]	I/O	SC BLK In	
22-P2[4]	I/O	Ext AGnd	
23-P2[6]	I/O	Analog Vref	
24-P0[0]	I/O	Analog Column In	ADC In
25-P0[2]	I/O	Analog Column In	ADC In
26-P0[4]	I/O	Analog Column In	ADC In
27-P0[6]	I/O	Analog Column In	ADC In

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C24X23A

Family can have up to three IO ports that connect to the global digital and analog interconnects, providing access to 4 digital blocks and 6 analog blocks. A switch mode pump(SMP) is added which allows running down to 1.0 volt battery supply.

CY8C24123A 8-Pin PSoC Device PDIP and SOIC

	VDD	GRD	ISSP	GPIO
Pin	8	4	3,5	Port 0(6,2,7,1) Port 1(5,3)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[5]	I/O	Analog Column In	Analog Column Out
2-P0[3]	I/O	Analog Column In	Analog Column Out
3-P1[1]	ISSP CLK*	I2C CLK	Ext Crystal In
5-P1[0]	ISSP DATA*	I2C Data	Ext Crystal Out
6-P0[2]	I/O	Analog Column In	
7-P0[4]	I/O	Analog Column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C24223A 20-Pin PSoC Device PDIP, SSOP, and SOIC

	VDD	GRD	ISSP	SMP	Reset	GPIO
Pin	20	10	9,11	5	15	Port 0(16,4,17,3,18,2,19,1) Port 1(11,9,12,8,13,7,14,6)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[7]	I/O	Analog Column In	
2-P0[5]	I/O	Analog Column In	Analog Col Out
3-P0[3]	I/O	Analog Column In	Analog Col Out
4-P0[1]	I/O	Analog Column In	
6-P1[7]	I/O	I2C CLK	
7-P1[5]	I/O	I2C Data	
9-P1[1]	ISSP CLK*	I2C CLK	Ext Crystal In
11-P1[0]	ISSP DATA*	I2C Data	Ext Crystal Out
13-P1[4]	I/O	EXT CLK IN	
16-P0[0]	I/O	Analog Column In	
17-P0[2]	I/O	Analog Column In	
18-P0[4]	I/O	Analog Column In	
19-P0[6]	I/O	Analog Column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C24423A 28-Pin PSoC Device PDIP, SSOP, and SOIC

	VDD	GRD	ISSP	Reset	SMP	GPIO
Pin	28	14	13,15	19	9	Port 0(24,4,25,3,26,2,27,1) Port 1(15,13,16,12,17,11,18,10) Port 2(20,8,21,7,22,6,23,5)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[7]	I/O	Analog Column In	
2-P0[5]	I/O	Analog Column In	Analog Column Out
3-P0[3]	I/O	Analog Column In	Analog Column Out
4-P0[1]	I/O	Analog Column In	
7-P2[3]	I/O	SC BLK In	
8-P2[1]	I/O	SC BLK In	
10-P1[7]	I/O	I2C SCL	
11-P1[5]	I/O	I2C SDA	
13-P1[1]	ISSP CLK*	I2C SCL	XTALin
15-P1[0]	ISSP DATA*	I2C SDA	XTALout
17-P1[4]	I/O	Ext Clk In	
20-P2[0]	I/O	SC BLK In	
21-P2[2]	I/O	SC BLK In	
22-P2[4]	I/O	Ext AGnd	
23-P2[6]	I/O	Analog Vref	
24-P0[0]	I/O	Analog Column In	
25-P0[2]	I/O	Analog Column In	
26-P0[4]	I/O	Analog Column In	
27-P0[6]	I/O	Analog Column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C24423A 32-Pin PSoC Device 32-Pin QFN or Sawn

Pin	VDD	GRD	ISSP	Reset	SMP	GPIO
	28	5,12	11,13	18	6	Port 0(23,32,24,31,26,30,27,29) Port 1(13,11,14,10,15,8,17,7) Port 2(19,4,20,3,21,2,22,1)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
3-P2[3]	I/O	Analog Column In	Direct SC Blk In
4-P2[1]	I/O	Analog Column In	Direct SC Blk In
7-P1[7]	I/O	I2C SCL	
8-P1[5]	I/O	I2C SDA	
11-P1[1]	ISSP CLK*	I2C SCL	XTALin
13-P1[0]	ISSP DATA*	I2C SDA	XTALout
15-P1[4]	I/O	EXT CLK IN	
19-P2[0]	I/O	Direct SC Blk In	
20-P2[2]	I/O	Direct SC Blk In	
21-P2[4]	I/O	Analog Grd Ref	
22-P2[6]	I/O	Ext Vref	
23-P0[0]	I/O	Analog column In	
24-P0[2]	I/O	Analog column In	
26-P0[4]	I/O	Analog column In	
27-P0[6]	I/O	Analog column In	
29-P0[7]	I/O	Analog column In	
30-P0[5]	I/O	Analog column In	Analog column Out
31-P0[3]	I/O	Analog column In	Analog column Out
32-P0[1]	I/O	Analog column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C24000A 56-Pin PSoC Device

The 56-pin SSOP part is for the CY8C24000A On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production. See datasheet for pin out information as this part does not have the same foot print as any of the CY8C24X23A parts.

CY8C24X94

These PSoC devices are unique members of the PSoC family because it includes a full-featured, full-speed (12 Mbps) USB port. The PSoC CY8C24x94 devices can have up to seven IO ports that connect to the global digital and analog interconnects, providing access to 4 digital blocks and 6 analog blocks. The Analog Mux Bus can connect to every GPIO pin in ports 0-5. Pins can be connected to the bus individually or in any

combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array. Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing.

CY8C24794 56-Pin PSoC Device QFN

	VDD	GRD	ISSP	USB	GPIO
Pin	49,22	50,19	18,25	20,21	Port 0(45,54,46,53,47,52,48,51)** Port 1(25,18,26,17,27,16,28,15)** Port 2(41,2,42,1,43,56,44,55)** Port 3(33,10,34,9,35,8,36,7)** Port 4(37,6,38,5,39,4,40,3)** Port5(29,14,30,13,31,12,32,11)** Port7(24,23)

**note: The Analog Mux Bus can connect to every GPIO pin in ports 0-5. Pins can be connected to the bus individually or in any combination.

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2nd Alternate
1-P2[3]	I/O	SC Blk In	
2-P2[1]	I/O	SC Blk In	
15-P1[7]	I/O	I2C SCL	
16-P1[5]	I/O	I2C SDA	
18-P1[1]	ISSP CLK*	I2C SCL	
25-P1[0]	ISSP DATA*	I2C SDA	
41-P2[0]	I/O	SC Blk In	
42-P2[2]	I/O	SC Blk In	
43-P2[4]	I/O	AGRN In	
44-P2[6]	I/O	VREF In	
45-P0[0]	I/O	Analog column In	
46-P0[2]	I/O	Analog column In	
47-P0[4]	I/O	Analog column In VREF	
48-P0[6]	I/O	Analog column In	
51-P0[7]	I/O	Analog column In	
52-P0[5]	I/O	Analog column In	Analog Column Out
53-P0[3]	I/O	Analog column In	Analog Column Out
54-P0[1]	I/O	Analog column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C24894 56-Pin PSoC Device QFN

The 894 device has a external reset function pin added in place of P3[6].

	VDD	GRD	ISSP	USB	RESET	GPIO
Pin	49,22	50,19	18,25	20,21	36	Port 0(45,54,46,53,47,52,48,51)** Port 1(25,18,26,17,27,16,28,15)** Port 2(41,2,42,1,43,56,44,55)** Port 3(33,10,34,9,35,8,NA,7)** Port 4(37,6,38,5,39,4,40,3)** Port5(29,14,30,13,31,12,32,11)** Port7(24,NA,NA,NA,NA,NA,NA,23)

**note: The Analog Mux Bus can connect to every GPIO pin in ports 0-5. Pins can be connected to the bus individually or in any combination.

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P2[3]	I/O	SC Blk In	
2-P2[1]	I/O	SC Blk In	
15-P1[7]	I/O	I2C SCL	
16-P1[5]	I/O	I2C SDA	
18-P1[1]	ISSP CLK*	I2C SCL	
25-P1[0]	ISSP DATA*	I2C SDA	
41-P2[0]	I/O	SC Blk In	
42-P2[2]	I/O	SC Blk In	
43-P2[4]	I/O	AGRN In	
44-P2[6]	I/O	VREF In	
45-P0[0]	I/O	Analog column In	
46-P0[2]	I/O	Analog column In	
47-P0[4]	I/O	Analog column In VREF	
48-P0[6]	I/O	Analog column In	
51-P0[7]	I/O	Analog column In	
52-P0[5]	I/O	Analog column In	Analog Column Out
53-P0[3]	I/O	Analog column In	Analog Column Out
54-P0[1]	I/O	Analog column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C24994 68-Pin PSoC Device QFN

Pin	VDD	GRD	ISSP	USB	RESET	GPIO
	23,59	7,20,60	19,32	21,22	46	Port 0(55,64,56,63,57,62,58,61)**
						Port 1(32,19,33,18,34,17,35,16)**
						Port 2(51,68,52,67,53,66,54,65)**
						Port 3(40,11,41,10,42,9,43,8)**
						Port 4(47,4,48,3,49,2,50,1)**
						Port5(36,15,37,14,38,13,39,12)**
						Port7(31,30,29,28,27,26,25,24)

**note: The Analog Mux Bus can connect to every GPIO pin in ports 0-5. Pins can be connected to the bus individually or in any combination.

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
16-P1[7]	I/O	I2C SCL	
17-P1[5]	I/O	I2C SDA	
19-P1[1]	ISSP CLK*	I2C SCL	
32-P1[0]	ISSP DATA*	I2C SDA	
34-P1[4]	I/O	EXT CLK In	
51-P2[0]	I/O	SC Blk In	
52-P2[2]	I/O	SC Blk In	
53-P2[4]	I/O	AGRN In	
54-P2[6]	I/O	VREF In	
55-P0[0]	I/O	Analog column In	
56-P0[2]	I/O	Analog column In	Analog Column Out
57-P0[4]	I/O	Analog column In	Analog Column Out
58-P0[6]	I/O	Analog column In	
61-P0[7]	I/O	Analog column In	Cint In #1
62-P0[5]	I/O	Analog column In	Cint In #2 or Analog Column Out
63-P0[3]	I/O	Analog column In	Analog Column Out
64-P0[1]	I/O	Analog column In	
67-P2[3]	I/O	SC Blk In	
68-P2[1]	I/O	SC Blk In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C24094 68-Pin OCD PSoC Device QFN

The 094 part has a on chip debugger on board. The pin out is the same as the 894 part with the addition of 4 control signals needed for real time debugging. These four pins used for OCD are no connects on the 894 device. The pins are pin 5-OCDE OCD even data IO, pin 6-OCDO OCD odd data output, pin 44-HCLK OCD high-speed clock output, and pin-45 CCLK OCD CPU clock output.

CY8C24994 PSoC device 100-ball VFBGA

	VDD	GRD	ISSP	USB	RESET	GPIO
Pin	A6,B6	A1,A2	G5,G6	J3,J4	F9	Port 0(C7,B4,B7,D5,D6,C5,C6,B5)**
	J5,K5	A9,A10				Port 1(G6,G5,H6,H5,H7,H4,G7,G4)**
		B1,B2,B9				Port 2(C8,B3,B8,E4,E7,D4,D7,C4)**
		B10,E5,E6				Port 3(F8,H3,H8,G3,G8,F3,E9,D2)**
		F5,F6,J1,J2				Port 4(D9,C2,C9,E3,E8,D3,D8,C3)**
		J9,J10,K1,K2				Port5(F7,F4,J8,H2,H9,G2,G9,F2)**
		K9,K10				Port7(J7,F10,G10,H10,K8,K7,K6,J6)

**note: The Analog Mux Bus can connect to every GPIO pin in ports 0-5. Pins can be connected to the bus individually or in any combination.

Some pins have shared resources that may be configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
G4-P1[7]	I/O	I2C SCL	
H4-P1[5]	I/O	I2C SDA	
G5-P1[1]	ISSP CLK*	I2C SCL	
G6-P1[0]	ISSP DATA*	I2C SDA	
H7-P1[4]	I/O	EXT CLK In	
C8-P2[0]	I/O	SC Blk In	
B8-P2[2]	I/O	SC Blk In	
E7-P2[4]	I/O	AGRN In	
D7-P2[6]	I/O	VREF In	
C7-P0[0]	I/O	Analog column In	
B7-P0[2]	I/O	Analog column In	Analog Column Out
D6-P0[4]	I/O	Analog column In	Analog Column Out
C6-P0[6]	I/O	Analog column In	
B5-P0[7]	I/O	Analog column In	Cint In #1
C5-P0[5]	I/O	Analog column In	Cint In #2 or Analog Column Out
D5-P0[3]	I/O	Analog column In	Analog Column Out
B4-P0[1]	I/O	Analog column In	
E4-P2[3]	I/O	SC Blk In	
B3-P2[1]	I/O	SC Blk In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C24094 On-Chip Debug (OCD) device 100-pin VFBGA not for production

The 094 part has a on chip debugger on board. The pin out is the same as the 994 part with the addition of 4 control signals needed for real time debugging. These four pins used for OCD are no connects on the 994 device. The pins are pin F1-OCDE OCD even data IO, pin G1-OCDO OCD odd data output, pin E10-HCLK OCD high-speed clock output, and pin-D10 CCLK OCD CPU clock output.

CY8C27X43

The PSoC CY8C27x43 family can have up to five IO ports that connect to the global digital and analog interconnects, providing access to 8 digital blocks and 12 analog blocks. The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements.

CY8C27143 8-Pin PSoC Device PDIP

	VDD	GRD	ISSP	GPIO
Pin	8	4	3,5	Port 0(NA,NA,6,2,7,1) Port 1(5,3)

Some pins have shared resources that may be configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2nd Alternate
1-P0[5]	I/O	Analog Column In	Analog Column Out
2-P0[3]	I/O	Analog Column In	Analog Column Out
3-P1[1]	ISSP CLK	I2C CLK	Xtal In
5-P1[0]	ISSP DATA	I2C Data	Xtal Out
6-P0[2]	I/O	Analog Column In	Analog Column Out
7-P0[4]	I/O	Analog Column In	Analog Column Out

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C27243 20-Pin PSoC Device (SSOP, SOIC)

	VDD	GRD	ISSP	SMP	Reset	GPIO
Pin	20	10	9,11	5	15	Port 0(16,4,17,3,18,2,19,1) Port 1(11,9,12,8,13,7,14,6)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[7]	I/O	Analog Col In	
2-P0[5]	I/O	Analog Col In	Analog Col Out
3-P0[3]	I/O	Analog Col In	Analog Col Out
4-P0[1]	I/O	Analog Col In	
6-P1[7]	I/O	I2C CLK	
7-P1[5]	I/O	I2C Data	
9-P1[1]	ISSP CLK	I2C CLK	Ext Crystal In
11-P1[0]	ISSP DATA	I2C Data	Ext Crystal Out
13-P1[4]	I/O	EXT CLK IN	
16-P0[0]	I/O	Analog Col In	
17-P0[2]	I/O	Analog Col In	Analog Col Out
18-P0[4]	I/O	Analog Col In	Analog Col Out
19-P0[6]	I/O	Analog Col In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C27443 28-Pin PSoC Device (PDIP, SSOP, SOIC)

	VDD	GRD	ISSP	Reset	SMP	GPIO
Pin	28	14	13,15	19	9	Port 0(24,4,25,3,26,2,27,1) Port 1(15,13,16,12,17,11,18,10) Port 2(20,8,21,7,22,6,23,5)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[7]	I/O	Analog Column In	
2-P0[5]	I/O	Analog Column In	Analog Column Out
3-P0[3]	I/O	Analog Column In	Analog Column Out
4-P0[1]	I/O	Analog Column In	
7-P2[3]	I/O	SC BLK In	
8-P2[1]	I/O	SC BLK In	
10-P1[7]	I/O	I2C SCL	
11-P1[5]	I/O	I2C SDA	
13-P1[1]	ISSP CLK*	I2C SCL	XTALin
15-P1[0]	ISSP DATA*	I2C SDA	XTALout
17-P1[4]	I/O	Ext Clk In	
20-P2[0]	I/O	SC BLK In	
21-P2[2]	I/O	SC BLK In	
22-P2[4]	I/O	Ext AGnd	
23-P2[6]	I/O	Analog Vref	
24-P0[0]	I/O	Analog Column In	
25-P0[2]	I/O	Analog Column In	Analog Column Out
26-P0[4]	I/O	Analog Column In	Analog Column Out
27-P0[6]	I/O	Analog Column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C27543 44-Pin PSoC Device (TQFP)

Pin	VDD	GRD	ISSP	Reset	SMP	GPIO
	39	17	16,18	26	8	Port 0(35,43,36,42,37,41,38,40) Port 1(18,16,19,15,20,14,21,13) Port 2(31,3,32,2,33,1,34,44) Port 3(22,12,23,11,24,10,25,9) Port 4(27,7,28,6,29,5,30,4)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
2-P2[3]	I/O	Analog Column In	Direct SC Blk In
3-P2[1]	I/O	Analog Column In	Direct SC Blk In
13-P1[7]	I/O	I2C SCL	
14-P1[5]	I/O	I2C SDA	
16-P1[1]	ISSP CLK*	I2C SCL	XTALin
18-P1[0]	ISSP DATA*	I2C SDA	XTALout
20-P1[4]	I/O	EXT CLK IN	
31-P2[0]	I/O	Direct SC Blk In	
32-P2[2]	I/O	Direct SC Blk In	
33-P2[4]	I/O	Analog Grd Ref In	
34-P2[6]	I/O	Ext Vref In	
35-P0[0]	I/O	Analog column In	
36-P0[2]	I/O	Analog column In	Analog column Out
37-P0[4]	I/O	Analog column In	Analog column Out
38-P0[6]	I/O	Analog column In	
40-P0[7]	I/O	Analog column In	
41-P0[5]	I/O	Analog column In	Analog column Out
42-P0[3]	I/O	Analog column In	Analog column Out
43-P0[1]	I/O	Analog column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C27643 48-Pin PSoC Device (SSOP)

	VDD	GRD	ISSP	RESET	SMP	GPIO
Pin	48	24	23,25	35	13	Port 0(44,4,45,3,46,2,47,1) Port 1(25,23,26,22,27,21,28,20) Port 2(40,8,41,7,42,6,43,5) Port 3(31,17,32,16,33,15,34,14) Port 4(36,12,37,11,38,10,39,9) Port5(29,19,30,18)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[7]	I/O	Analog column In	
2-P0[5]	I/O	Analog column In	Analog column Out
3-P0[3]	I/O	Analog column In	Analog column Out
4-P0[1]	I/O	Analog column In	
7-P2[3]	I/O	Analog Column In	Direct SC Blk In
8-P2[1]	I/O	Analog Column In	Direct SC Blk In
20-P1[7]	I/O	I2C SCL	
21-P1[5]	I/O	I2C SDA	
23-P1[1]	ISSP CLK*	I2C SCL	XTALin
25-P1[0]	ISSP DATA*	I2C SDA	XTALout
27-P1[4]	I/O	EXT CLK IN	
40-P2[0]	I/O	Direct SC Blk In	
41-P2[2]	I/O	Direct SC Blk In	
42-P2[4]	I/O	Analog Grd Ref In	
43-P2[6]	I/O	Ext Vref In	
44-P0[0]	I/O	Analog column In	
45-P0[2]	I/O	Analog column In	Analog column Out
46-P0[4]	I/O	Analog column In	Analog column Out
47-P0[6]	I/O	Analog column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C27643 48-Pin PSoC Device (QFN)

Pin	VDD	GRD	ISSP	RESET	SMP	GPIO
	42	18	17,19	29	7	Port 0(38,46,39,45,40,44,41,43) Port 1(19,17,20,16,21,15,22,14) Port 2(34,2,35,1,36,48,37,47) Port 3(25,11,26,10,27,9,28,8) Port 4(30,6,31,5,32,4,33,3) Port5(23,13,24,12)

Some pins have shared resources that may be configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[7]	I/O	Analog column In	
2-P0[5]	I/O	Analog column In	Analog column Out
3-P0[3]	I/O	Analog column In	Analog column Out
4-P0[1]	I/O	Analog column In	
7-P2[3]	I/O	Analog In	Direct SC Blk In
8-P2[1]	I/O	Analog In	Direct SC Blk In
20-P1[7]	I/O	I2C SCL	
21-P1[5]	I/O	I2C SDA	
23-P1[1]	ISSP CLK*	I2C SCL	XTALin
25-P1[0]	ISSP DATA*	I2C SDA	XTALout
27-P1[4]	I/O	EXT CLK IN	
40-P2[0]	I/O	Direct SC Blk In	
41-P2[2]	I/O	Direct SC Blk In	
42-P2[4]	I/O	Analog Grd Ref In	
43-P2[6]	I/O	Ext Vref In	
44-P0[0]	I/O	Analog column In	
45-P0[2]	I/O	Analog column In	Analog column Out
46-P0[4]	I/O	Analog column In	Analog column Out
47-P0[6]	I/O	Analog column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C27002 56-Pin ODC PSoC Device (SSOP)

The 56-pin SSOP part is for the CY8C27002 On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Four special OCD signals are brought out for real time debugging. Signals and pins listed below.

Pin-14 OCD OCDE OCD even data IO

Pin-15 OCD OCDO OCD odd data output

Pin-42 OCD HCLK OCD high-speed clock output

Pin-43 OCD CCLK OCD CPU clock output

	VDD	GRD	ISSP	USB	RESET	GPIO
Pin	49,22	50,19	18,25	20,21	36	Port 0(52,5,53,4,54,3,55,2) Port 1(31,27,32,26,33,24,34,23) Port 2(48,9,49,8,50,7,51,6) Port 3(37,20,38,19,39,18,40,17) Port 4(44,13,45,12,46,11,47,10) Port5(35,22,36,17)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
2-P0[7]	I/O	Analog column In	
3-P0[5]	I/O	Analog column In	Analog column Out
4-P0[3]	I/O	Analog column In	Analog column Out
5-P0[1]	I/O	Analog column In	
8-P2[3]	I/O	Analog column In	Direct SC Blk In
9-P2[1]	I/O	Analog column In	Direct SC Blk In
23-P1[7]	I/O	I2C SCL	
24-P1[5]	I/O	I2C SDA	
27-P1[1]	ISSP CLK*	I2C SCL	XTALin
31-P1[0]	ISSP DATA*	I2C SDA	XTALout
33-P1[4]	I/O	EXT CLK IN	
48-P2[0]	I/O	Direct SC Blk In	
49-P2[2]	I/O	Direct SC Blk In	
50-P2[4]	I/O	Analog Grd Ref In	
51-P2[6]	I/O	Ext Vref In	
52-P0[0]	I/O	Analog column In	
53-P0[2]	I/O	Analog column In	Analog column Out
54-P0[4]	I/O	Analog column In	Analog column Out
55-P0[6]	I/O	Analog column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C29X66

The PSoC CY8C29x66 family can have up to eight IO ports that connect to the global digital and analog interconnects, providing access to 16 digital blocks and 12 analog blocks. Memory encompasses 32 KB of Flash for program storage, 2 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

CY8C29466 28-Pin PSoC Device (PDIP, SSOP, SOIC)

	VDD	GRD	ISSP	Reset	SMP	GPIO
Pin	28	14	13,15	19	9	Port 0(24,4,25,3,26,2,27,1) Port 1(15,13,16,12,17,11,18,10) Port 2(20,8,21,7,22,6,23,5)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[7]	I/O	Analog Column In	
2-P0[5]	I/O	Analog Column In	Analog Column Out
3-P0[3]	I/O	Analog Column In	Analog Column Out
4-P0[1]	I/O	Analog Column In	
7-P2[3]	I/O	SC BLK In	
8-P2[1]	I/O	SC BLK In	
10-P1[7]	I/O	I2C SCL	
11-P1[5]	I/O	I2C SDA	
13-P1[1]	ISSP CLK*	I2C SCL	XTALin
15-P1[0]	ISSP DATA*	I2C SDA	XTALout
17-P1[4]	I/O	Ext Clk In	
20-P2[0]	I/O	SC BLK In	
21-P2[2]	I/O	SC BLK In	
22-P2[4]	I/O	Ext AGnd	
23-P2[6]	I/O	Analog Vref	
24-P0[0]	I/O	Analog Column In	
25-P0[2]	I/O	Analog Column In	Analog Column Out
26-P0[4]	I/O	Analog Column In	Analog Column Out
27-P0[6]	I/O	Analog Column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C29566 44-Pin PSoC Device (TQFP)

Pin	VDD	GRD	ISSP	Reset	SMP	GPIO
	39	17	16,18	26	8	Port 0(35,43,36,42,37,41,38,40) Port 1(18,16,19,15,20,14,21,13) Port 2(31,3,32,2,33,1,34,44) Port 3(22,12,23,11,24,10,25,9) Port 4(27,7,28,6,29,5,30,4)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
2-P2[3]	I/O	Analog column In	Direct SC Blk In
3-P2[1]	I/O	Analog column In	Direct SC Blk In
13-P1[7]	I/O	I2C SCL	
14-P1[5]	I/O	I2C SDA	
16-P1[1]	ISSP CLK*	I2C SCL	XTALin
18-P1[0]	ISSP DATA*	I2C SDA	XTALout
20-P1[4]	I/O	EXT CLK IN	
31-P2[0]	I/O	Direct SC Blk In	
32-P2[2]	I/O	Direct SC Blk In	
33-P2[4]	I/O	Analog Grd Ref In	
34-P2[6]	I/O	Ext Vref In	
35-P0[0]	I/O	Analog column In	
36-P0[2]	I/O	Analog column In	Analog column Out
37-P0[4]	I/O	Analog column In	Analog column Out
38-P0[6]	I/O	Analog column In	
40-P0[7]	I/O	Analog column In	
41-P0[5]	I/O	Analog column In	Analog column Out
42-P0[3]	I/O	Analog column In	Analog column Out
43-P0[1]	I/O	Analog column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C29666 48-Pin PSoC Device (SSOP)

Pin	VDD	GRD	ISSP	RESET	SMP	GPIO
	48	24	23,25	35	13	Port 0(44,4,45,3,46,2,47,1) Port 1(25,23,26,22,27,21,28,20) Port 2(40,8,41,7,42,6,43,5) Port 3(31,17,32,16,33,15,34,14) Port 4(36,12,37,11,38,10,39,9) Port 5(29,19,30,18)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P0[7]	I/O	Analog column In	
2-P0[5]	I/O	Analog column In	Analog column Out
3-P0[3]	I/O	Analog column In	Analog column Out
4-P0[1]	I/O	Analog column In	
7-P2[3]	I/O	Analog column In	Direct SC Blk In
8-P2[1]	I/O	Analog column In	Direct SC Blk In
20-P1[7]	I/O	I2C SCL	
21-P1[5]	I/O	I2C SDA	
23-P1[1]	ISSP CLK*	I2C SCL	XTALin
25-P1[0]	ISSP DATA*	I2C SDA	XTALout
27-P1[4]	I/O	EXT CLK IN	
40-P2[0]	I/O	Direct SC Blk In	
41-P2[2]	I/O	Direct SC Blk In	
42-P2[4]	I/O	Analog Grd Ref In	
43-P2[6]	I/O	Ext Vref In	
44-P0[0]	I/O	Analog column In	
45-P0[2]	I/O	Analog column In	Analog column Out
46-P0[4]	I/O	Analog column In	Analog column Out
47-P0[6]	I/O	Analog column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C29666 48-Pin PSoC Device (QFN)

Pin	VDD	GRD	ISSP	RESET	SMP	GPIO
	42	18	17,19	29	7	Port 0(38,46,39,45,40,44,41,43) Port 1(19,17,20,16,21,15,22,14) Port 2(34,2,35,1,36,48,37,47) Port 3(25,11,26,10,27,9,28,8) Port 4(30,6,31,5,32,4,33,3) Port5(23,13,24,12)

Some pins have shared resources that maybe configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
1-P2[3]	I/O	Direct SC Blk In	
2-P2[1]	I/O	Direct SC Blk In	
14-P1[7]	I/O	I2C SCL	
15-P1[5]	I/O	I2C SDA	
17-P1[1]	ISSP CLK*	I2C SCL	XTALin
19-P1[0]	ISSP DATA*	I2C SDA	XTALout
21-P1[4]	I/O	EXT CLK IN	
34-P2[0]	I/O	Direct SC Blk In	
35-P2[2]	I/O	Direct SC Blk In	
36-P2[4]	I/O	Analog Grd Ref In	
37-P2[6]	I/O	Ext Vref In	
38-P0[0]	I/O	Analog column In	
39-P0[2]	I/O	Analog column In	Analog column Out
40-P0[4]	I/O	Analog column In	Analog column Out
41-P0[6]	I/O	Analog column In	
43-P0[7]	I/O	Analog column In	
44-P0[5]	I/O	Analog column In	Analog column Out
45-P0[3]	I/O	Analog column In	Analog column Out
46-P0[1]	I/O	Analog column In	

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C29866 100-Pin PSoC Device (TQFP)

Pin	VDD	GRD	ISSP	RESET	SMP	GPIO
	32,82,83	15,34,65	30,44	62	14	Port 0(74,3,77,99,79,97,81,95)
						Port 1(44,30,45,29,46,28,47,24)
						Port 2(68,7,69,6,70,5,72,4)
						Port 3(56,19,57,18,58,17,59,16)
						Port 4(63,11,64,10,66,9,67,8)
						Port 5(52,23,53,22,54,21,55,20)
						Port 6(86,87,88,89,90,91,92,93)
						Port 7(43,42,41,40,39,38,37,36)

Some pins have shared resources that may be configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
3-P0[1]	I/O	Analog column In	
6-P2[3]	I/O	Direct SC Blk In	
7-P2[1]	I/O	Direct SC Blk In	
24-P1[7]	I/O	I2C SCL	
28-P1[5]	I/O	I2C SDA	
30-P1[1]	ISSP CLK*	I2C SCL	XTALin
44-P1[0]	ISSP DATA*	I2C SDA	XTALout
46-P1[4]	I/O	EXT CLK IN	
68-P2[0]	I/O	Direct SC Blk In	
69-P2[2]	I/O	Direct SC Blk In	
70-P2[4]	I/O	Analog Grd Ref In	
72-P2[6]	I/O	Ext Vref In	
74-P0[0]	I/O	Analog column In	
77-P0[2]	I/O	Analog column In	Analog column Out
79-P0[4]	I/O	Analog column In	Analog column Out
81-P0[6]	I/O	Analog column In	
95-P0[7]	I/O	Analog column In	
97-P0[5]	I/O	Analog column In	Analog column Out
99-P0[3]	I/O	Analog column In	Analog column Out

* note: CLK and DATA pins are not high impedance at POR, used for ISSP

CY8C29000 On-Chip Debug (OCD) PSoC device

Note This part is only used for in-circuit debugging. It is NOT available for production. Four special OCD signals are brought out for real time debugging. Other Debug signals and pins listed below.

Pin-12 OCDE OCD even data IO	Pin-29 P1[3] I FMTEST,	Pin-79 P0[4] VREF
Pin-13 OCDO OCD odd data output	Pin-30 P1[1] TC SCLK	
Pin-60 HCLK OCD high speed clock output	Pin-44 P1[0] TC SDATA	
Pin-61 CCLK OCD CPU clock output	Pin-45 P1[2] V FMTEST	

Pin	VDD	GRD	ISSP	RESET	SMP	GPIO
	32,82,83	15,34,65 84,85	30,44	62	14	Port 0(74,3,77,99,79,97,81,95) Port 1(44,30,45,29,46,28,47,24) Port 2(68,7,69,6,70,5,72,4) Port 3(56,19,57,18,58,17,59,16) Port 4(63,11,64,10,66,9,67,8) Port 5(52,23,53,22,54,21,55,20) Port 6(86,87,88,89,90,91,92,93) Port 7(43,42,41,40,39,38,37,36)

Some pins have shared resources that may be configured for alternate functions. These pins are listed below with the alternate functions.

Pin	Primary	Alternate	2 nd Alternate
3-P0[1]	I/O	Analog column In	
6-P2[3]	I/O	Direct SC Blk In	
7-P2[1]	I/O	Direct SC Blk In	
24-P1[7]	I/O	I2C SCL	
28-P1[5]	I/O	I2C SDA	
30-P1[1]	ISSP CLK*	I2C SCL	XTALin
44-P1[0]	ISSP DATA*	I2C SDA	XTALout
46-P1[4]	I/O	EXT CLK IN	
68-P2[0]	I/O	Direct SC Blk In	
69-P2[2]	I/O	Direct SC Blk In	
70-P2[4]	I/O	Analog Grd Ref In	
72-P2[6]	I/O	Ext Vref In	
74-P0[0]	I/O	Analog column In	
77-P0[2]	I/O	Analog column In	Analog column Out
79-P0[4]	I/O	Analog column In	Analog column Out
81-P0[6]	I/O	Analog column In	
95-P0[7]	I/O	Analog column In	
97-P0[5]	I/O	Analog column In	Analog column Out
99-P0[3]	I/O	Analog column In	Analog column Out

* note: CLK and DATA pins are not high impedance at POR, used for ISSP