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Introduction

Multicore processors have earned a reputation for high performance. Many design engineers assume that raising the performance bar also boosts power consumption and price.

The TMS320C6472 from Texas Instruments challenges those assumptions by offering remarkable power efficiency for affordable solutions in a range of applications.

Powered by six TMS320C64x+™ DSP cores, the C6472 consumes only 60 percent of the power and occupies 80 percent less board space than six TMS320C6415 DSPs.

At 3.7 watts per device, it offers even greater power savings compared to general-purpose processors (GPUs) in the same performance range. In addition to its inherent advantage in signal processing, the C6472 can also keep up with GPUs in most generic control-oriented applications. Applications include but are by no means limited to multimedia server blades, voice conferencing, medical imaging, industrial machine vision, military-aerospace, and test and measurement.

Low power consumption and a competitive price tag make the six-core **TMS320C6472** ideal for high-performance applications

As more multicore-based systems make their way into high-performance applications, the advantages of multicore architectures are becoming more widely appreciated by the design community.

Most of the benefits spring from the opportunity to parallelize and share the system's computational load. Dividing tasks that must be executed more or less concurrently between multiple cores allows the functionality to reside within a smaller number of devices, each running at a lower clock rate. In such instances, multicore devices as a whole consume less energy than a combination of single-core devices, which must run much faster to execute the same tasks. In many instances, a multicore processor outperforms a single-core device running at three or four times the clock rate. This results in impressive power/performance ratios, including power efficiencies similar to TI's C55x™ devices, remarkable cost and footprint reductions, and better ease of use.

Through integration and by running cooler, multicore devices reduce the cost of packaging. To the degree that the cores share I/O, memory and other functional blocks, they reduce the silicon cost as well. Reduced system clocks also make it possible to fabricate the chips in a more mature, less expensive silicon process technology. Compared to a system that utilizes discrete processors for each of the cores in a multicore device, enormous savings can be achieved in board space.

Systems based on multicore devices are not new. But many earlier implementations have failed to achieve the performance gains – or market success – originally anticipated by system designers. This can usually be traced to the failure to fully utilize the parallelization opportunities multicore architectures provide. This, in turn, can often be traced to an architecture that locks software developers into a specific implementation. Software development is almost invariably the big issue.

In some cases, marketing goals bump up against reality. In other words, Amdahl's Law, which states that everything cannot be divided into parallel tasks, comes into play. But more frequently, code has not been tweaked and optimized for parallel processing, and this is especially true for embedded systems where careful coding always makes a big difference. TI successfully addresses these considerations in the C6472, with a more generic implementation that focuses on shared memory and avoids the complexity and inflexibility of previous multicore implementations.

Today's leading-edge, high-performance applications can be divided into three broad categories: applications that drive many channels; applications that demand maximum performance density; and breakthrough applications for which designers must have access to sophisticated functions. Some applications will span more than one of these categories.

The newest requirement for multicore is that this performance and functionality come with much lower power consumption and a low price tag. Making low power consumption a high priority for systems that are not battery-powered may seem counterintuitive. But minimizing power dissipation is often critical for high-performance systems that are housed in confined spaces where high ambient temperatures lead to reduced performance or even failure. In fact, all high-performance systems have power budgets and are cost-sensitive, particularly as subsystem design teams adopt a full-system optimization perspective.

Although the C6472 is among TI's highest performance DSPs, it also features low power consumption and competitive pricing. Six C64x+™ DSP cores, 4.8 MB of on-chip memory and an optimized DSP architecture combine to deliver up to the equivalent of 4.2-GHz performance. The three speed options – 500/625/700 MHz – deliver 24,000, 30,000 and 33,600 (16-bit) MMAC performance, respectively. The C6472 consumes 0.15 mW/MIPS at 3 GHz and has a low entry point price.

It offers a rich set of peripherals including Gigabit Ethernet, sRIO, DDR2, TSIP, HPI, Utopia, I2C, timer and GPIO.

Architectural overview

Because it is based on the C64x+ core, which achieved one of Berkeley Design Technology Inc.'s (BDTI) highest speed scores, the C6472 has 100 percent backward compatibility with other C64x DSPs. This enables legacy code reuse and faster time to market. In most instances, however, it would be a mistake simply to reuse code or just optimize it for multicore processing. For the best possible performance, the code should be optimized for parallel processing. In high-performance embedded applications, design teams invariably need to obtain the best possible performance.

Improved inter-core communication and a field-proven memory architecture combine to optimize CPU performance. Instead of forcing a specific “all out” approach to symmetric multicore architecture, only key enhancements such as shared memory and event aggregation were added. This keeps the architecture neutral, making it more manageable for embedded processing. For high-density, multichannel applications, designers found that it is easier to approach the maximum use of all six cores on the C6472.

The C6472 uses an architecture similar to previous TI devices, which have proven their performance and power efficiency primarily in communications infrastructure applications. Large on-chip memories help eliminate the need for external memory, thereby reducing system power dissipation and system cost and optimizing board density. Figure 1 shows the C6472's major functional blocks.

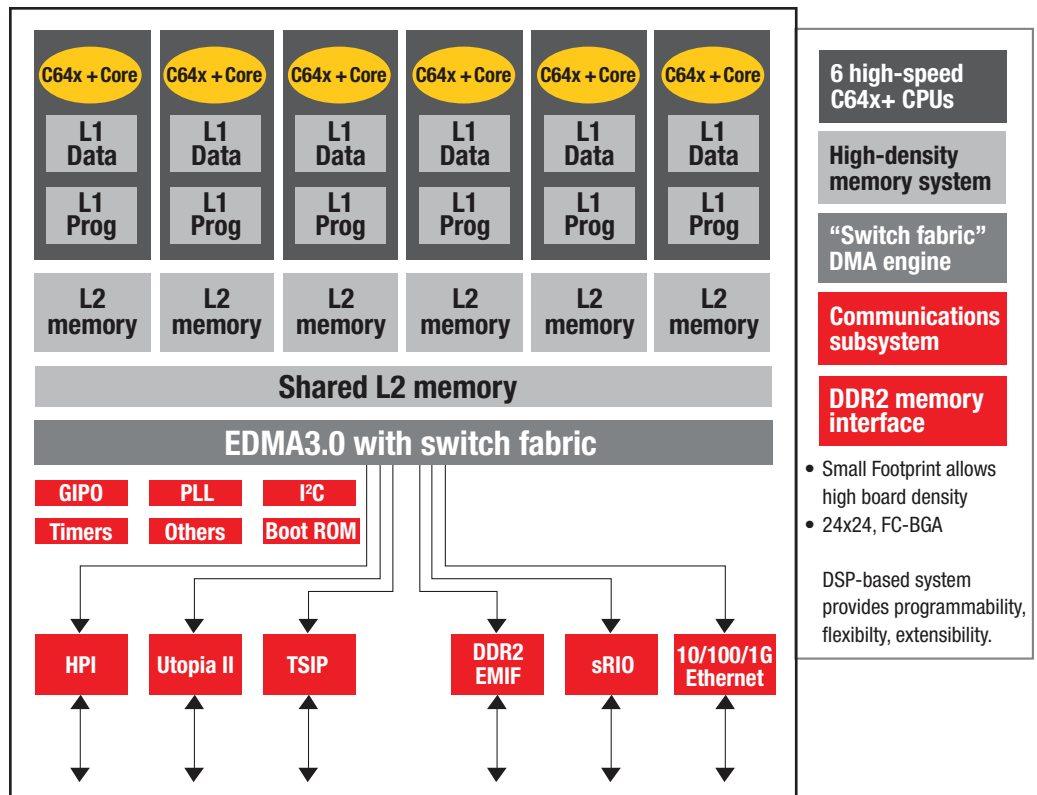


Figure 1: Integrating the EDMA with the switch fabric speeds up communication with memory and peripherals.

Memory access performance is an important feature of this architecture. In addition to L1 and L2 memory dedicated to each core, the six cores also share 768 KB of L2 memory. Shared L2 memory is managed by a separate controller and can be configured as either program or data memory. The 608 KB of unified L2 memory that is dedicated to each core is just as flexible. It can be utilized as either program or data memory and, if used for data, it can be configured as cache. There is 32 KB of L1 program memory and 32 KB of L1 data memory, which can also be configured as cache.

Performance is also enhanced by very tightly connecting the EDMA and the switch fabric into a single functional unit. This creates a fast connection to memory and peripherals that can maintain high throughput to those CPUs and peripherals that have high data bandwidths. The switch fabric uses several techniques to maximize throughput, not the least of which is handling multiple concurrent transfers. The architecture also allows communications peripherals to initiate data transfers without CPU intervention, which saves cycles and increases overall communications performance.

A carefully selected set of communications peripherals supports specific applications: UTOPIA 2 for telecommunications, 10/100/1G Ethernet for IP networks, and Serial RapidIO for DSP-to-DSP communications. Serial RapidIO® interfaces can connect directly to the DSP or through the switch fabric. The TDM ports can handle as many as 3,072 timeslots and a host port has been designed to accommodate a DSP memory probe.

The external memory interface (EMIF) supports the DDR2 standard to provide a low-cost option in today's memory market. Configured for 8- or 16-bit transfers, DDR memories can run at data rates specified by the standard between 400 and 533 MHz.

As mentioned earlier, the cooler running six-core C6472 can be accommodated in a less expensive package. In some instances, one board can replace two, which provides a significant cost reduction. In addition, the small footprint of the 24-by-24-mm FC-BGA package allows more room for other chips, which helps boost raw performance.

In an independent analysis for certain non-traditional DSP applications such as control processing or blade server segments, the C6472 boosted performance by an order of magnitude compared to GPU-based chips while staying within industry-standard power profiles, such as those for ATCA and uTCA.

The results of a benchmark analysis by VirtualLogix in Figure 2 show that a single-core C6472 delivers the best power/performance metrics of the chips tested, which allows systems to run cooler and boards to be packed more densely.

BYTEmark is a benchmark suite created by BYTE magazine that uses algorithm-level tests. In Figure 2, memory (MEM) and integer (INT) performance are compared for four processors. In the case of TI DSPs, a single core was tested to normalize the comparison because the processors do not have the same number of cores. Note also that the cores run at different speeds, with the TMS320C6474 running at about twice the speed of the other three processors. This has an effect on the raw performance figures. The other three processors provide roughly equivalent raw performance, but this is not the most important consideration in power-constrained applications.

The two columns on the right in the table measure power efficiency by dividing the raw performance benchmark (for MEM and INT) by the power consumed.

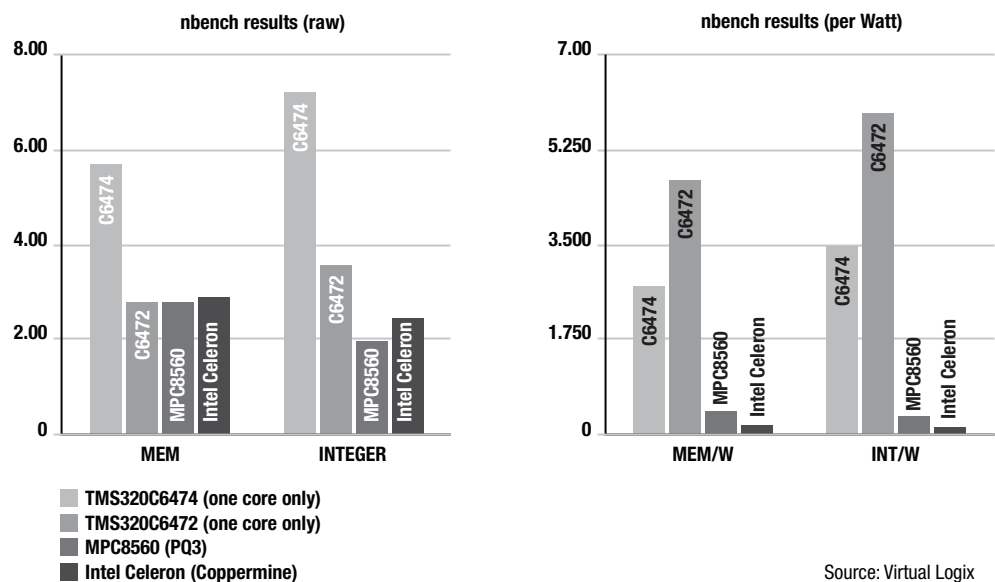
TI DSP BYTE nBench results

BYTEmark is a benchmark suite with algorithm level tests from BYTE Magazine.

The two indices (MEM and INT) are a measurement of memory efficiency and integer performance.

Processor	MHz	W	MEM	INTEGER	MEM/W	INT/W
TMS320C6474 (one core only)	1000	2.05	5.758	7.281	2.803	3.545
TMS320C6472 (one core only)	500	0.60	2.880	3.634	4.776	6.027
MPC8560 (PQ3)	660	6.40	2.869	2.012	0.448	0.314
Intel Celeron (Coppermine)	638	20.00	2.922	2.515	0.146	0.126

MEM and INTEGER values are indexes based on a AMD K6/233



Source: Virtual Logix

Figure 2: BYTE nBench BYTEmark normalized results.

In very high performance applications that are also power-constrained, DSPs can perform very well, even for applications that predominately call on control functions. One reason for this is that as GPU and DSP architectures have evolved, the pipeline lengths of both architectures have tended to converge. In the past, DSPs had longer pipelines that reduced performance.

The benchmark tests used Standard C code running on top of Linux. The suite is widely used and includes the following functions: numeric sort, string sort, bit fields, floating-point emulation, Fourier, assignment, idea, Huffman, neural net and LU decomposition tests.

Software development

Particularly for embedded systems, developing optimized code that is parallelized for execution on a multicore processor is essential to success. Although the concept of effortlessly retargeting linear code to a multiprocessor system using code generation is an attractive idea, it is not realistic.

TI supplies C6472-specific tools and an ecosystem of third-party partners that eliminates many of the time-to-market barriers usually associated with developing optimized code.

Support begins with the low-cost C6472 evaluation module (EVM), which includes Code Composer Studio™ version 4 (CCSv4) and its multicore processor capabilities. This version is a major upgrade based on the Eclipse open-source software framework, which is becoming a standard framework for embedded software vendors. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debugging capabilities from TI. The result is a compelling, feature-rich development environment for embedded developers.

The EVM also includes a driver for TI's XDS100 emulator, an ultra-low-cost USB-interface JTAG hardware reference design. Hardware is manufactured by TI third parties such as Sundance, Surf, Radisys and elfochips.

Software development tools available include a math library, a signal processing library, image library, floating-point emulation, BIOS/NDK and a chip support library. Software partners in the C6472 ecosystem include ADT and ENEA.

Applications

Raw processing power and an abundance of parallel processing paths make the C6472 a good choice for applications that drive many channels, as well as applications that demand maximum power/performance. Breakthrough applications for which designers must have access to sophisticated functions are also good candidates.

Wireless communication tester

A new generation of wireless communications testers is closer to home for a multicore DSP device because of its association with cellular base stations. These all-in-one testers combine the functionality required for a base station tester, a mobile user equipment tester, a base station service area tester, and technology-specific versions of standard T&M equipment such as digital signal generators and logic analyzers.

The primary advantage of using C6472 devices to design these high-end testers is the number of channels that can be accommodated by multicore devices. Data is easily parallelized, signal processing is essential, and it is much easier to design a system in which power consumption is kept within reasonable limits.

The ability to program the device on the fly is also essential because as a multifunction system, the tester must implement a very large number of functions, including but certainly not limited to:

- Protocol testing
- Real-time measurement and analysis of multipath, fading, interference, Doppler effect
- Radio wave propagation characterization of BTS
- Field strength, delay profile, noise, channel power, precision return loss
- Distance to fault, spectrum analysis, Tx/Rx characteristics

High-end automated inspection

Image processing typically requires a great deal of processing power. High-end automated inspection systems using machine vision are pushing the performance envelope even further, particularly in the semiconductor industry.

The image requirements of wafer inspection systems, for example, include very high resolution and frame rates. Many of these systems also use multiple cameras, which increases the required channel capacity. It is not atypical for a high-end system to generate 10 megapixel images and run at frame rates between 120 and 300 frames per second. Even larger images are required for the inspection of solar cells and larger wafers.

The list of required functionalities of automated testers is just as impressive. These included image preconditioning and noise reduction, image enhancement, 2-D/3-D filtering, edge detection, defect identification and frequency domain analysis.

C6472-based systems execute these features with great efficiency because of their inherent signal-processing capability. Almost as important is the C6472's ability to handle many channels, especially when multiple cameras are in use. High-end machine inspection is applied in facilities other than wafer processing plants. When multiple systems are in use on a large factory floor, the low-power advantages of the C6472 can result in large cost savings.

Ultrasound nondestructive testing

Ultrasound can be used as a noninvasive probing technology in both medical and industrial applications. The high level of detail in the resulting images is obtained by a phased array of ultrasound transmitters that are pulsed in sequence to produce a steerable, tightly focused, high-resolution beam.

This technique produces a high-resolution image showing a slice through the object. The phased-array data that is received by sensors requires up to 256 channels, each operating at between 2 and 20 MHz. To produce the desired images, a typical ultrasound system produces images of slightly less than 1 MB per frame, must operate at 20 frames per second, and attain a delay of less than 50 ms.

Signal processing is central to the technology and includes steering and focusing the beam, signal preconditioning, noise reduction, scan conversion, post-processing and frequency domain analytics.

C6472-based systems would provide both the number of channels and the signal-processing performance required by a high-end ultrasound tester.

Conclusion

As high-performance applications demand the availability of more channels and more processing power, systems based on multicore devices are gaining popularity. Power consumption and device cost have always been a concern. TI's six-core C6472 challenges these assumptions by offering low-power, affordable solutions for a range of applications. Independent benchmarks indicate that the C6472 can compete with general-purpose processors, especially when taking power consumption into consideration.

To help optimize multicore development, TI has provided extensive support for the C6472, including an evaluation module, libraries and a third-party ecosystem.

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