



DK-DEV-2AGX125N

Texas Instruments Powers Altera's Arria II GX FPGA Development Kit

Arria® II GX FPGAs are low-cost FPGAs with high-end capabilities and 3.75 Gb/s transceivers. Designed for cost-sensitive applications, Arria II GX FPGAs are based on a 40 nm, full-featured FPGA fabric that includes Adaptive Logic Modules (ALMs), DSP blocks, embedded RAM and a hard PCIe IP core. Unlike other comparable FPGAs with high-speed transceivers, Arria II GX FPGAs offer a host of high-end features like DSP blocks, a high multiplier-to-logic ratio, a high memory-to-logic ratio, and design security, as well as improvements in usability to enable designers to complete their projects faster.

TI's power solution used on the Arria II GX development platform offers many features that benefit engineers in their final designs. Integration of components and voltage rails decrease board space and make overall design easier. Examples of this in the design are integrated-FET DCDC converters (TPS54617, TPS62510) and dual-channel DCDC controllers and linear regulators (TPS40140, TPS71202). Linear regulators offer simple design and low-noise output voltages. The TPS74801 and TPS74701 allow for extremely low-input voltages (0.8V) and low-dropout voltages (50 mV), resulting in high LDO efficiency, while still offering very low-noise outputs for sensitive analog circuitry ($25 \mu\text{V}_{\text{RMS}}/\text{V}_{\text{OUT}}$). Texas Instruments provides a complete, high-performance and cost-competitive solution to power Arria II GX FPGAs.



Development Kit Features

- Device: EP2AGX125EF35C5N
- PCIe SIG-compliant card
- Embedded USB-Blaster™ download cable
- Fast passive parallel configuration via Flash
- Push-buttons, LEDs
- Parallel Flash
- DDR2 SO-DIMM (x72 width)
- DDR3 device 8M x 16-bit x 8 banks
- SRAM 512K x 36-bit, 200 MHz
- Ethernet ASSP PHY
- Power measurement circuitry
- Two HSMC connectors
- SMA's (for clock inputs only)
- RJ-45 connector

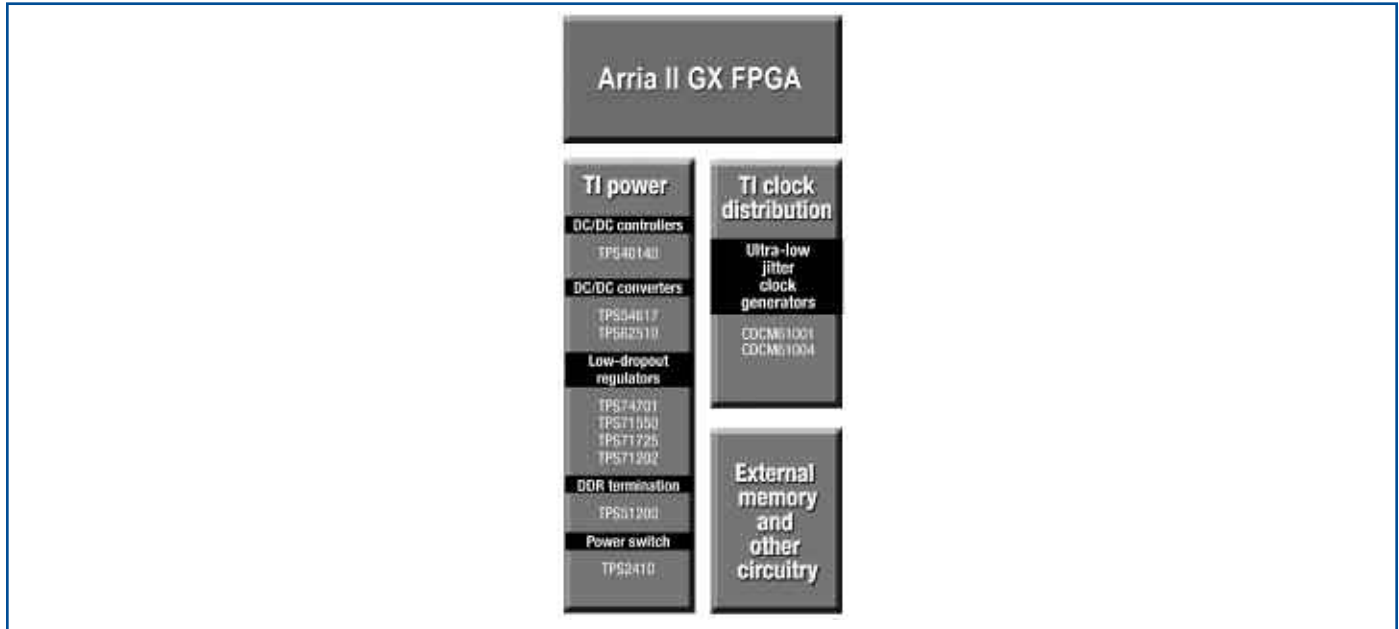
Arria II GX FPGAs Potential Applications

- PCIe Gen1 bridging
- Gigabit Ethernet
- Broadcast (Triple-rate SDI)
- Wireless 3G and LTE communications (CPRI, OBSAI, etc.)
- Wireline communications (DLSAM, GPON, EPON, Ethernet, SONET)

Arria II GX Development Kit



TI Power and Clock Distribution on Altera's Arria II GX Development Kit



TI Power and Clock Attach

Part Number	Description	Voltage	Voltage Pins/Domains or Clock Speed
TPS2410	N+1 and OR-ing power rail controller	12V and 3.3V	System 12V and 3.3V
TPS40140	Stackable 2-channel multiphase or 2-channel independent output controller	5.0V	5.0V, ENET_DVDD, Enet PHY DVDD A2VCC, A2GX core VCC
TPS54617	3V to 5V, 6A, 1.6 MHz step-down SWIFT converter	2.5V	2.5V, Sync SRAM, Flash VDDQ, Enet PHY AVDD, EPM2210, four oscillators, two clock buffers A2VCCIO_B3B_B5B_B6B, A2GX260 Banks 3B, 5B, and 6B VCCIO A2VCCIO_B5A, A2GX bank 5A VCCIO A2VCCIO_B6A, A2GX bank 6 VCCIO A2VCCIO_B7B_B8A, A2GX banks 7B and 8A VCCIO A2VCCPD, A2GX VCCPD
TPS54617	3V to 5V, 6A, 1.6 MHz step-down SWIFT converter	1.8V	1.8V, DDR2 SODIMM, Flash VDD, EPM2210 VCCINT A2VCCIO_B3A_B4, A2GX banks 3A and 4
TPS62510	Adjustable, 97% efficiency, 1.5A buck converter for low-input voltages	1.5V	1.5V, DDR3 VDD/VDDQ A2VCCIO_B7A, A2GX bank 7A VCCIO
TPS74701	Single output LDO, 500 mA, adj (0.8V to 3.6V), programmable soft start	1.1V	A2VCCL_GXB, A2GX GXB PMA/clocking
TPS74701	Single output LDO, 500 mA, adj (0.8V to 3.6V), programmable soft start	1.0V	ENET_DVDD, Enet PHY DVDD
TPS74801	Single output LDO, 1.5A, adj (0.8V to 3.6V), programmable soft start	1.5V	A2VCCH_GXB, A2GX transceiver VCCH_GXB A2VCCB, A2GX config RAM bits
TPS71550	Single output LDO, 50 mA, fixed (5.0V), high-input voltage, low-quiescent current	5.0V	5.0V_MONITOR
TPS71725	Single output LDO, 150 mA, fixed (2.5V), high PSRR, low-quiescent current, low-noise	2.5V	A2VCCA, A2GX GXB PMA A2VCCA_PLL, A2GX analog PLL
TPS71202	Dual 250 mA output, ultra low-noise, high PSRR, low dropout linear regulator	3.3V	3.3V_USB, EPM240Z VCCIO emb., blaster, USB PHY IO, 24M OSC, AT93C46DN, EEPROM M2Z_VCCINT, EPM240Z VCCINT
TPS51200	Sink/source DDR termination regulator	0.9V	0.9V_VTT and 0.9V_VREF, DDR3 ADDR/CMD term and ref
TPS51200	Sink/source DDR termination regulator	0.75V	0.75V_VTT and 0.75V_VREF, DDR2 ADDR/CMD term and ref
CDCM61001	1:1 ultra-low jitter crystal-in clock generator	-	100 MHz
CDCM61004	1:4 ultra-low jitter crystal-in clock generator	-	125 MHz

For more information, such as datasheets and app notes, visit www.arrow.com/arrowedge.