



EP4S40G2/5 and EP4S100G2/3/4/5

Stratix® IV GT FPGAs with 11.3 Gb/s Transceivers

The Stratix® IV GT FPGAs feature serial transceivers that support data rates between 2.488 Gb/s and 11.3 Gb/s. Stratix IV GT FPGAs are members of Altera's 40 nm Product Portfolio along with Stratix IV GX, Stratix IV E and Arria II GX FPGAs, and HardCopy IV and HardCopy IV GX ASICs.

Stratix IV GT FPGAs can be broadly classified into the following categories:

- FPGAs targeted at applications that need to achieve 40 Gb/s ingress/egress data rates
- FPGAs targeted at applications that need to achieve 100 Gb/s ingress/egress data rates

Applications

- Wireline communications
 - 40G/100G MACs/framers
 - Ethernet aggregation
 - Bridging functions
 - Packet processing
 - Traffic management
- Military
- Test and medical
- Proprietary 10G applications

Protocols

10G independent channels

- 10 Gb Ethernet
- 10 Gb Fibre Channel
- Sonet/SDH OC-192
- G.709 OTU-2

40G bonded channels

- Interlaken
- SPAUI, DDR-XAUI
- 40G IEEE 802.3ba, XLAUI
- SFI-4.2/SFI-5.1/SFI-5.2/SFI-S
- MLD

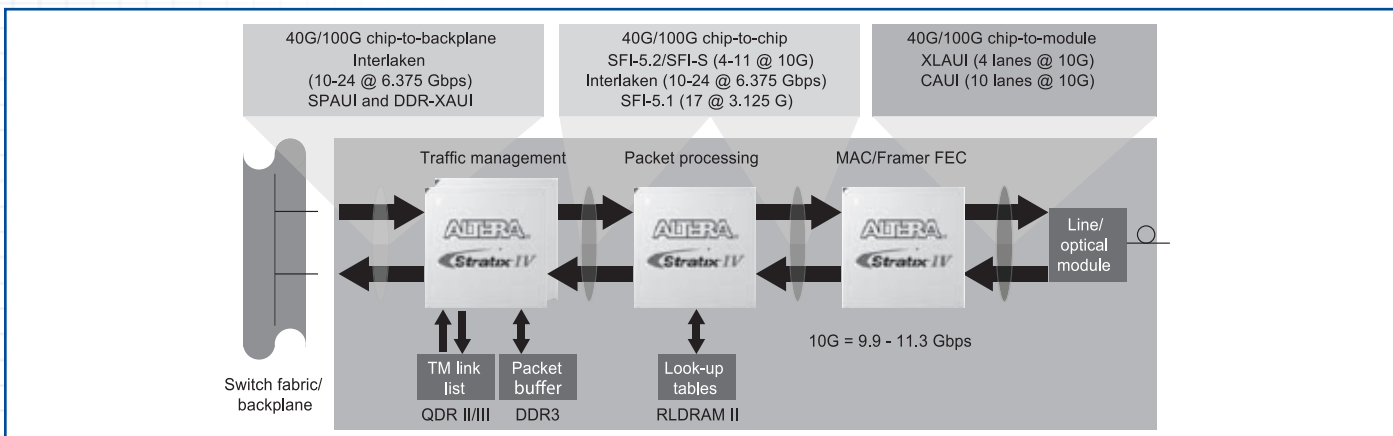
100G bonded channels

- Interlaken
- SPAUI, DDR-XAUI
- 100G IEEE 802.3ba, CAUI
- SFI-S
- MLD

Though optimized for 40 Gb/s and 100 Gb/s systems, Stratix IV GT transceivers also provide support for the following protocols:

- PCI Express Gen1 and Gen2
 - Including a complete protocol solution with embedded PCI Express hard IP blocks that implement PHY-MAC layer, Data Link layer, and Transaction layer functionality
- Gigabit Ethernet
- SONET/SDH (OC-48, OC-96)
- XAUI/HiGig
- (OIF) CEI PHY interface
- Fibre Channel
- 10G/6G/3G basic modes, enable proprietary protocols

40G/100G Line Card with Stratix IV GT FPGAs



Additional Transceiver Features

Low power

Typical Physical Medium Attachment (PMA) power consumption per channel¹:

- 100 mW at 3.125 Gb/s
- 135 mW at 6.375 Gb/s
- 165 mW at 8.5 Gb/s
- 190 mW at 10.3 Gb/s
- 200 mW at 11.3 Gb/s

¹ Power numbers are preliminary, pending full device characterization

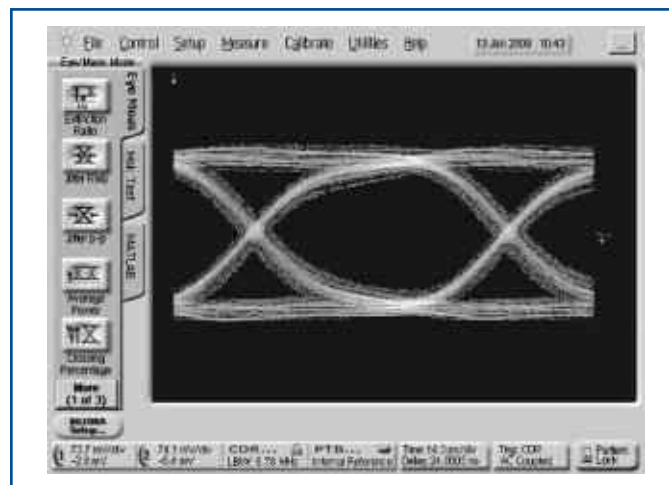
Signal integrity

Stratix IV GT FPGAs simplify the challenge of signal integrity through a number of chip, package, and board-level enhancements to enable efficient high-speed data transfer. These enhancements include:

- Programmable transmitter pre-emphasis
- User-controlled and adaptive receiver equalization

- On-die regulators for transmitter and receiver Phase-Locked Loop (PLL) charge pump and Voltage Controlled Oscillator (VCO) power supplies for superior noise immunity
- On-package and on-chip power supply decoupling which reduces the need for on-board decoupling capacitors

11.3 Gb/s Eye Diagram



Stratix IV GT FPGAs Features

Feature	EP4S40G2	EP4S40G5	EP4S100G2	EP4S100G3 ¹	EP4S100G4 ¹	EP4S100G5	
Package pin count	1517	1517	1517	1932	1932	1517	1932
ALMs	91,200	212,480	91,200	116,480	141,440	212,480	
LEs	228,000	531,200	228,000	291,200	353,600	531,200	
Total transceiver channels	36	36	36	48	48	36	48
10G transceiver channels (2.488 Gb/s to 11.3 Gb/s)	12	12	24	24	24	24	24
8G transceiver channels (2.488 Gb/s to 8.5 Gb/s) ⁵	12	12	0	8	8	0	8
PMA-only CMU channels (2.488 Gb/s to 6.5 Gb/s)	12	12	12	16	16	12	16
High-speed LVDS SERDES (up to 1.6 Gb/s)	44	44	44	44	44	44	44
SP1-4.2 links	2	2	2	2	2	2	2
M9K blocks (256 × 36 bits)	1,235	1,280	1,235	936	1,248	1,280	
M144K blocks (2048 × 72 bits)	22	64	22	36	48	64	
Total memory (MLAB + M9K + M144K) Kb	17,133	27,376	17,133	17,248	22,564	27,376	
Embedded multipliers 18 × 18 ²	1,288	1,024	1,288	832	1,024	1,024	
PLLs	8	12	8	12	12	8	12
User I/Os ^{3,4}	636	636	636	754	754	636	754

Notes

¹ The Quartus II software version 9.0 does not support EP4S100G3 and EP4S100G4. These devices will be supported in a future release of the Quartus II software.

² Four multiplier adder mode.

³ The total number of user I/Os does not include the high-speed transceiver I/Os and dedicated configuration pins. Dedicated clock pins are included.

⁴ User I/O count is preliminary, subject to change.

⁵ All 10G transceiver channels can also be configured as 8G transceiver channels. For example, the EP4S40G2F40 device has twenty-four 8G transceiver channels and the EP4S100G5F45 device has thirty-two 8G transceiver channels.

For more information, such as datasheets and app notes, visit www.arrow.com/arrowedge.