



ADSP-21469

High-Performance Floating-Point DSP

The ADSP-21469 SHARC® processor is a member of the SIMD SHARC family of DSPs that features Analog Devices' Super Harvard architecture.

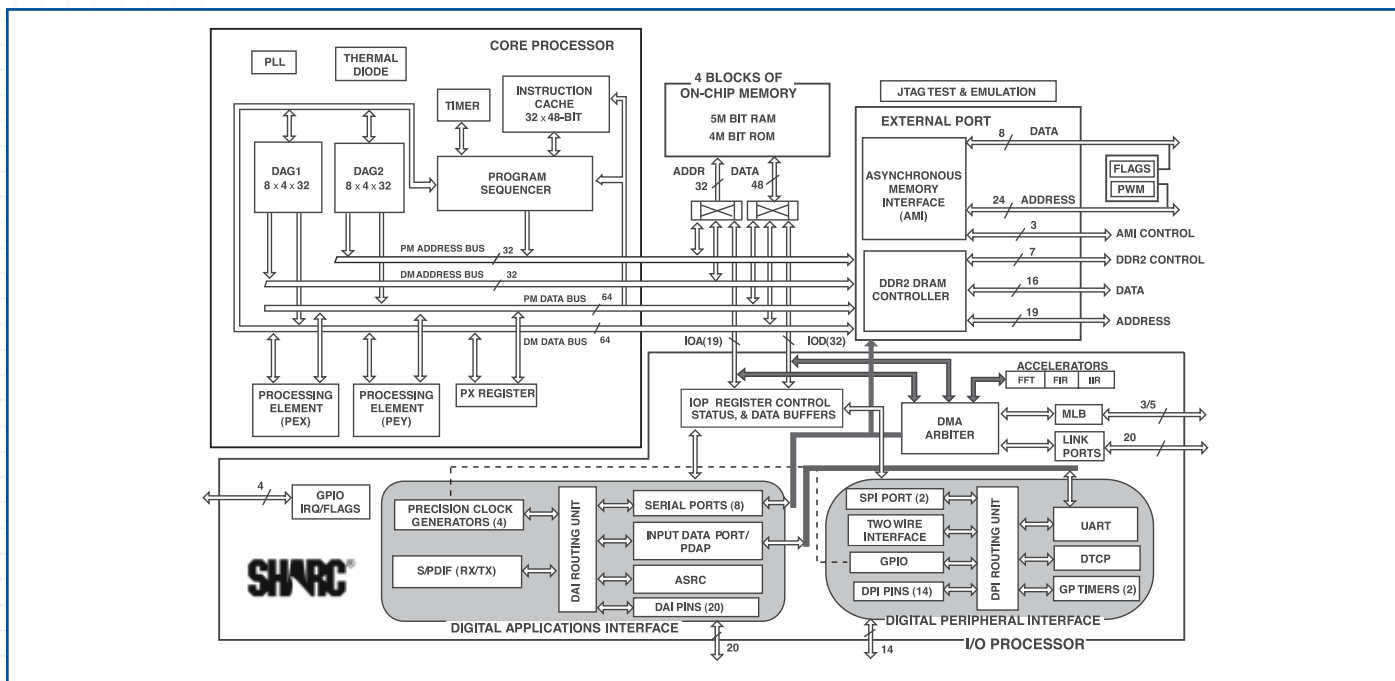
The processor is source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. This new processor is a 32-bit/40-bit floating point processor optimized for high performance audio applications with its large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative Digital Applications Interface (DAI).

The ADSP-2146x processor is available with unique audiocentric peripherals such as the digital applications interface, Digital Transmission Content Protection (DTCP) protocol, serial ports, precision clock generators, S/PDIF transceiver, asynchronous sample rate converters, input data port, and more.

Features

- At up to 450 MHz core instruction rate, the processor performs at 2.7 GFLOPS/900 MMACs
- 5 Mb on-chip RAM, 4 Mb on-chip ROM for simultaneous access by the core processor and DMA
- DDR2 DRAM interface (16-bit) operating at maximum frequency of half the core clock frequency
- Dual Data Address Generators (DAGs) with modulo and bitreverse addressing
- Transfers between memory and core at a sustained 7.2 GB/s bandwidth
- Two 8-bit wide link ports can connect to the link ports of other SHARCs or peripherals. Link ports are bidirectional programmable ports having eight data lines, an acknowledge line and a clock line
- DMA controller supports up to 67 DMA channels for transfers between internal memory and a variety of peripherals
- 16-bit data access for synchronous DDR2 DRAM memory
- 8-bit data access for asynchronous memory
- Four memory select lines allows multiple external memory devices
- DAI includes eight serial ports, four precision clock generators, an input data port, an S/PDIF transceiver, and a signal routing unit
- Four independent Asynchronous Sample Rate Converters (ASRC)
- TDM support for telecommunications interfaces
- Pulse-width modulation provides: 16 PWM outputs configured as four groups of four outputs supports center-aligned or edge-aligned PWM waveforms
- PLL has a wide variety of software and hardware multiplier/divider ratios

Functional Block Diagram



SHARC Family Features

Feature	ADSP-21462W	ADSP-21465W	ADSP-21467	ADSP-21469	ADSP-21469W
Frequency (CCLK)	400 MHz	400 MHz	450 MHz	450 MHz	400 MHz
RAM	5 Mb	5 Mb	5 Mb	5 Mb	5 Mb
ROM ¹	N/A	4 Mb	4 Mb	N/A	N/A
Audio decoders in ROM	No	Yes	Yes	No	No
Pulse-width modulation	Yes	Yes	Yes	Yes	Yes
S/PDIF	Yes	Yes	Yes	Yes	Yes
DTCP ²	Yes	Yes	No	No	No
DDR2 memory interface	1/2 CCLK Max	1/2 CCLK Max	1/2 CCLK Max	1/2 CCLK Max	1/2 CCLK Max
DDR2 memory bus width	16 bits	16 bits	16 bits	16 bits	16 bits
Direct DMA from SPORTs to external memory	Yes	Yes	Yes	Yes	Yes
FIR accelerator	Yes	Yes	Yes	Yes	Yes
IIR accelerator	Yes	Yes	Yes	Yes	Yes
FFT accelerator	Yes	Yes	Yes	Yes	Yes
MLB interface	Yes	Yes	No	No	Yes
IDP	Yes	Yes	Yes	Yes	Yes
Serial ports	8	8	8	8	8
SRU	2	2	2	2	2
DDR2 memory interface	Yes	Yes	Yes	Yes	Yes
UART	1	1	1	1	1
DAI and DPI	20/14 pins	20/14 pins	20/14 pins	20/14 pins	20/14 pins
Link ports	2	2	2	2	2
S/PDIF transceiver	1	1	1	1	1
AMI interface with 8-bit support	Yes	Yes	Yes	Yes	Yes
SPI	2	2	2	2	2
TWI	Yes	Yes	Yes	Yes	Yes
Package	324-ball PBGA	324-ball PBGA	324-ball PBGA	324-ball PBGA	324-ball PBGA
SRC performance	128 dB	128 dB	128 dB	128 dB	128 dB

¹ Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Prologic II, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations.

² The ADSP-21462W and ADSP-21465W processors provide the Digital Transmission Content Protection protocol, a proprietary security protocol.

For more information, such as datasheets and app notes, visit www.arnowac.com/arrowedge.