



AD9251/9268

Dual 14-/16-Bit 80/125 MSPS 1.8V
High-Speed A/D Converters

The AD9251 is a monolithic, dual-channel 1.8V supply, 14-bit, 20/40/65/80 MSPS A/D converter, featuring a high-performance sample-and-hold circuit and on-chip voltage reference.

The product uses a multistage differential pipeline architecture with output error correction logic to provide 14-bit accuracy at 80 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The A/D converter contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the Serial Port Interface (SPI).

The AD9251 is available in a 64-lead LFSCP and is specified over the industrial temperature range (-40°C to +85°C).

The AD9268 is a dual, 16-bit, 125 MSPS A/D converter. The AD9268 is designed to support communications applications where high-performance, combined with low-cost, small size, and versatility, is desired.

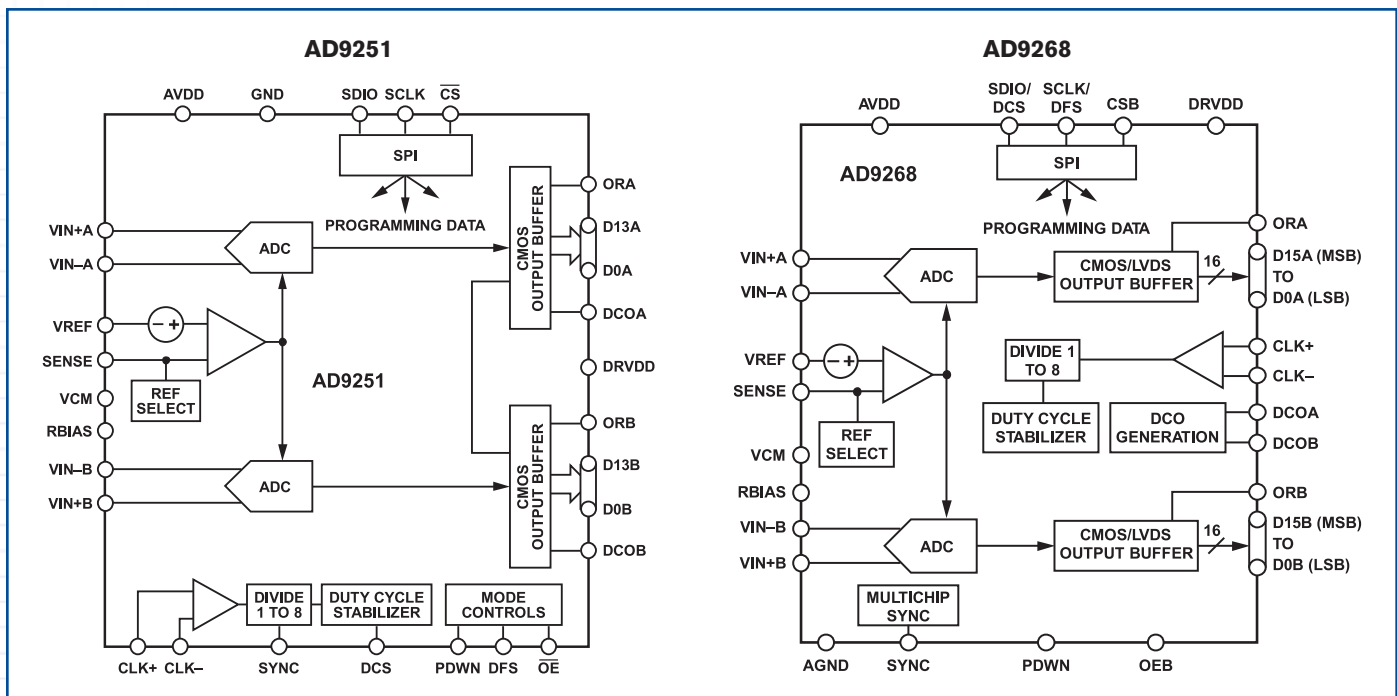
The dual A/D converter core features a multistage, differential pipelined architecture with integrated output error correction logic. Each A/D converter features wide-bandwidth, differential sample-and-hold analog input amplifiers that support a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the A/D converter clock duty cycle, allowing the converters to maintain excellent performance.

The A/D converter output data can be routed directly to the two external 16-bit output ports. These outputs can be set to either 1.8V CMOS or LVDS.

Flexible power-down options allow significant power savings, when desired.

The AD9268 is available in a 64-lead LFCSP and is specified over the industrial temperature range (-40°C to +85°C).

Functional Block Diagrams



AD9251 Features

- 1.8V analog supply operation
- 1.8V to 3.3V output supply
- SNR: 74 dBFS at 9.7 MHz input
- SFDR: 95 dBc at 9.7 MHz input
- SNR: 71.5 dBFS at 200 MHz input
- SFDR: 78 dBc at 200 MHz input
- Low-core power
- 35 mW/ch at 20 MSPS
- 70 mW/ch at 80 MSPS
- Differential input with 700 MHz bandwidth
- On-chip voltage reference and sample-and-hold circuit
- DNL = ± 0.5 LSB
- Flexible analog input: $1V_{P-P}$ or $2V_{P-P}$ differential
- Offset binary, gray code, or twos complement data format
- Optional clock duty cycle stabilizer
- Integer 1-to-8 input clock divider
- Data clock out with programmable clock and data alignment
- Serial port control
- Built-in selectable digital test pattern generation
- Energy-saving power-down modes

Applications

- Communications
- Diversity radio systems
- Multimode digital receivers
- GSM, EDGE, WCDMA, LTE, CDMA2000, WiMAX, TD-SCDMA
- I/Q demodulation systems
- Smart antenna systems
- Ultrasound equipment

AD9251

- Battery-powered instruments
- Hand-held scope meters
- Radar/LIDAR

AD9268

- Broadband data applications
- General-purpose software radios

AD9268 Features

- SNR = 78.2 dBFS at 70 MHz
- SFDR = 88 dBc at 70 MHz
- Low-power: 750 mW at 125 MSPS
- 1.8V analog supply operation
- 1.8V CMOS or LVDS output supply
- Integer 1-to-8 input clock divider
- IF sampling frequencies to 300 MHz
- -153.6 dBm/Hz small-signal input noise with 200Ω input impedance at 70 MHz and 125 MSPS
- Optional on-chip dither
- Programmable internal A/D converter voltage reference
- Integrated A/D converter sample-and-hold inputs
- Flexible analog input range: $1V_{P-P}$ to $2V_{P-P}$
- Differential analog inputs with 650 MHz bandwidth
- A/D converter clock duty cycle stabilizer
- 95 dB channel isolation/crosstalk
- Serial port control
- User-configurable, Built-In Self-Test (BIST) capability
- Energy-saving power-down modes

For more information, such as datasheets and app notes, visit www.arrow.com/arrowedge.