

Micrel Creates Fail-Safe Input for Use in High-Bandwidth Clock and Data Distribution ICs

Solution eliminates need for external termination resistors between the source and destination.

To achieve the lowest jitter, lowest skew, and fastest clock and data distribution in a system, designers have long utilized differential signaling technology such as LVPECL, CML, or LVDS. More recently, IC suppliers have begun to offer more innovative solutions in this product space with new features such as internal termination, blazing-fast edge rates, extremely low crosstalk-induced jitter, tiny packaging, and fail-safe inputs (FSI).

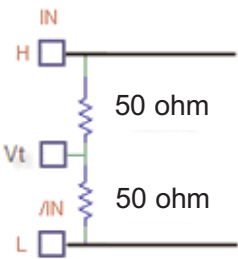


Figure 1. Three-pin internal termination.

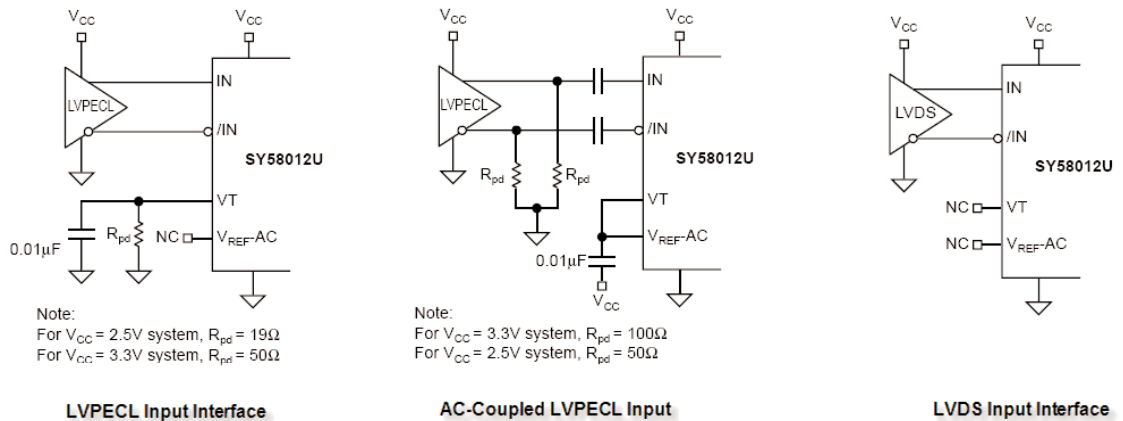
Figure 1 shows an example of a three-pin internal termination. In the past, external termination resistors had to be placed physically as close to the receiver as possible. This approach led to difficulties in layout, additional external components, parasitic capacitance and inductance, and, worst of all, stubs which caused reflections. To eliminate stubs and maximize signal integrity, Micrel has implemented a 3-pin internal termination in its Precision Edge® products, which allows termination of AC- or DC-coupled LVPECL, CML, or LVDS input signals. With this solution, no external termination resistors are required between the source and destination. Figure 2 shows various input termination schemes with this three-pin internal termination. Even with this solution, the question of what happens to the output when the input to a LVPECL, CML, or LVDS device is absent or greatly degraded still exists.

In the past, when the input to a LVPECL, CML, or LVDS device was absent or greatly degraded, there would be a metastable condition. The output would be in an undetermined state and even small amounts of noise at the input would cause the output to ring.

Prior to three-pin internal terminations, designers tried to compensate by changing the values of the external termination resistors so that a voltage offset would be present between IN and /IN when no input signal was present. This would produce a known output state when the input was absent. It was widely accepted, however, that this solution wasn't ideal because the introduction of the DC offset could, and often did, produce significant duty-cycle distortion during normal operation. For most designs, the duty-cycle distortion was enough to eliminate this approach as a feasible solution.

Micrel's SY58605U 3.2 Gb/s precision LVDS buffer, with internal termination and fail-safe input, specifies a 100 mV_{PK} maximum input voltage threshold that triggers FSI. In other words, when the input voltage differential drops sufficiently below 100 mV_{PK} (200 mV_{PP}), typically 30 mV_{PK}, then the output stops switching and remains in the last known valid state. The FSI function eliminates a metastable condition and guarantees a stable output. No ringing or undetermined state will occur at the output when the input clock or data fails to a floating, static, or extremely low signal swing. The IC guarantees operation over the full industrial temperature range (-40 degrees Celsius to +85 degrees Celsius) and is available in MLF® packaging, which features low inductance and capacitance, making it ideal for today's high-speed, low-jitter designs.

For more information or to download datasheets, visit www.arrow.com/resource, or call 800-241-3902.



Note:
For V_{CC} = 2.5V system, R_{pd} = 19Ω
For V_{CC} = 3.3V system, R_{pd} = 50Ω

Note:
For V_{CC} = 3.3V system, R_{pd} = 100Ω
For V_{CC} = 2.5V system, R_{pd} = 50Ω

Note: MLF is a registered trademark of Amkor Technology. PrecisionEdge is a registered trademark of Micrel, Inc.

Figure 2. Various input termination schemes using 3-pin internal termination.